A GENERAL DISCUSSION
of the
MIL-STD-1397C ( NAVY )
NTDS INTERFACE STANDARD
and the
MIL-STD-188-203-1A ( D2 )
ATDS SERIAL INTERFACE STANDARD

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SECTION 1
INTRODUCTION

1.1 THE NAVY TACTICAL DATA SYSTEM

The Navy Tactical Data System (NTDS) is based on the interaction of humans and machines. The NTDS helps coordinate fleet air defense, antisubmarine warfare, and surface defense operations. Through automation, the NTDS provides commanders with a broad picture of the current tactical situation and assists in directing operations in time to intercept potential enemy threats. The use of digital computers and digital data processing techniques reduces reaction time and increases force effectiveness.

1.2 A BRIEF HISTORY

In the later stages of World War II the Japanese began to abandon coordinated tight formation air attacks in favor of massed combined suicide and conventional attacks coming from all directions. These tactics created overwhelming amounts of lookout and radar tactical data that had to be processed manually in real time by the ships’ air defense coordinators. These tasks involved interpretation of radar data, identifying threats, relaying messages, and manually plotting the information on large plexiglass map display boards.

1.2.1 THE PROBLEM

During close range combat, the shipboard combat information center (CIC) is involved in complex tactical situations requiring important decisions to be made in a short period of time. The speed at which these combat situations must be solved is inconceivable to someone thinking in terms of typical human based CIC operations of the 1940’s. At times the sheer quantity of tactical data and reporting task complexity would overwhelm the plot crew causing data critical to the fleet defense to be late or lost.

1.2.2 THE SOLUTION

After performing task force battle assessments in the late 1940’s the Navy realized that it needed some new technology teamed with radar to help human users assimilate and interpret the massive amount of tactical data available from its new electronic radar and sonar sensor suites. The Navy Tactical Data System was conceived as an automated tool for assisting combat situation commanders in making rapid tactical decisions.

1.3 NTDS SYSTEM COMPONENTS

The NTDS consists of high-speed computers, data display consoles, communication links, and operational computer programs. The total system functions to collect, analyze, and correlate sensor data to obtain a clear picture of the tactical situation. A good tactical picture includes complete target data on all ships, aircraft, and submarines in the area of concern. This picture is then converted to digital format and supplied to the weapon systems of the ship and to other ships over the communications data link. Figure 1.1 shows the NTDS equipment grouping and how it interfaces with the weapons and ship sensor systems.
FIGURE 1.1
THE NTDS SYSTEM

FIGURE 1.2
THE LINKS
1.3.1 NTDS COMPUTERS

The first production NTDS suite was the AN/USQ-20(V) and consisted of an assemblage of peripheral equipment and computers, designated the CP-642. In 1959 the navy specified a tactical computer design which would be modular, powerful, and reliable. Thus the CP-642 with 30 bit instructions, fourteen 30 bit I/O channels, and 32k word memory was born. The first CP-642 was delivered in 1960 and production continued until 1975 for a total of 380 computers.

1.3.1.1 EQUIPMENT STANDARDIZATION

As part of the standardization strategy the Navy defined the physical and electrical interface between the various equipment in the AN/USQ-20(V) suite. This specification came to be MIL-STD-1397C (NAVI) Military Standard Document and defines several parallel and serial equipment interface types. The standardization equipment interface strategy proved so successful that it was adapted for use by the navies of many other countries. GET produces interface adaptor and emulation products that enable non-NTDS equipped computers and peripheral equipment to comply with these Navy standards.

1.3.2 COMMUNICATIONS SUBSYSTEM

NTDS uses three separate data transmission links to maintain tactical data communications between tactical units (Figure 1.2). Each link is able to transfer data to other ships, aircraft, and shore facilities without the delay of human interface. The data processing subsystem formats the messages for each of the data links. These messages are based on shipboard inputs from displays, sensors, and other data links.

1.3.2.1 LINK 11

Link 11 (TADIL A) is a secure link between NTDS-equipped surface ships. Link 11 provides high-speed, computer-to-computer transfer of tactical information, command orders, and unit status to all tactical data systems. The type of tactical information transferred is surface, subsurface, air, and track information and consists of friendly, hostile, and unknown identity tracks. The new Link-11/22, a member of the Joint Message Standard (TADIL-J) family, will improve Link-11 connectivity and reliability and will be the common data link for all Navy and allied ships not equipped with Link-16.

1.3.2.2 LINK 14

Link 14 provides a means of transmitting track information to those units not capable of participating in the Link 11 network. Instead of being displayed automatically, the information is presented in a Teletype format and must be manually plotted.

1.3.2.3 LINK 4A

Link 4A is a secure data link between surface units and aircraft and permits the computer to take control of the autopilot in an equipped aircraft. It may control a flight out to a strike area and return it to base without the need for pilot action. The pilot also has the option of using his visual display to aid in understanding the intercept controller, or to totally ignore and override the link 4A transmission.
1.3.2.4 LINK 16

Link 16 (JTIDS/TADIL J) is a secure tactical data system with an embedded digital voice channel and Tactical Air Navigation (TACAN) functions. The high data rate JTIDS link provides aircraft and ships with crypto secure, jam-resistant, and low-probability of exploitation communications capability. This high capacity system provides a secure, jam-resistant (via frequency hopping) link for voice communications, navigation, and tactical data, including secret information.

1.3.3 THE AEGIS SYSTEM

Over the years the NTDS has changed from a basic Combat Direction System (CDS) to the Advanced Combat Direction System (ACDS). The NTDS was originally considered an individual unit instead of a component of the combat system. The NTDS function is now being performed by the same equipment that performs other functions formerly not associated with NTDS. The AEGIS weapon system (Figure 1.3) is the first system designed under the one-system concept. The AEGIS Command and Decision (C&D) system not only performs the NTDS function but also controls the electronic warfare (EW) system, IFF challenges, and several other functions as well.

FIGURE 1.3
THE AEGIS COMBAT SYSTEM
SECTION 2
NTDS PARALLEL INTERFACE

2.1 SCOPE

The following discussion addresses the general design philosophy used in the design of GET NTDS Parallel Interface adaptors and supporting products and is intended to assist qualified personnel in their implementation and installation. It is not the intent or purpose of this document to define the actual uses or application of NTDS interface adaptors. Programming and application examples or diagrams which may be found in this document are intended only to illustrate the operation of the NTDS interface.

2.1.1 NTDS OVERVIEW

The NTDS interface was originally developed in the early 1960’s as a standardized point to point communications specification to be used between all Navy tactical computers and their peripheral devices. Four types of Parallel and two types of Serial data format systems are specified. The physical connection between compatible equipment is by means of a pair of cables. One cable is used to transfer Input Data and Interrupts while the other cable transfers Output Data and Commands. The individual transfers are performed using a strict Request / Acknowledge timing protocol. The connector types, contact assignments, and cable types are specified. Actual data and command word formats, applications, and actions invoked by the transactions are not addressed by the specification.

2.2 NTDS PARALLEL INTERFACE OVERVIEW

The GET NTDS Parallel Interface Adaptors can be configured to operate as NTDS Peripheral or Computer channel devices. Each CHANNEL consists of an Input PORT and an Output PORT, each containing up to 32 data lines and four control lines (Figure 2.2). The transfer of information by each port is conducted using these control lines. The following discussion is intended only as an aid in explaining a general operation of an NTDS Parallel Data channel and does not cover all aspects of the NTDS protocol. For a complete description of the NTDS protocols refer to MIL-STD-1397C (NAVY) Military Standard Document.

2.2.1 PARALLEL INTERFACES

There are four types of NTDS Parallel interfaces specified, each of which can operate in three Categories. The NTDS TYPE defines the electrical interface characteristics while the CATEGORY describes the signal timing protocol used for information exchange operations.

2.2.2 PARALLEL INTERFACE CATEGORIES

The GET NTDS parallel interface ports are individually configurable to operate as Computer or Peripheral channels. This enables a single interface adaptor to operate in any one of the three NTDS equipment categories defined in MIL-STD-1397C. These equipment categories are:

A. Category I - Computer to Peripheral
B. Category II - Computer to Computer (Inter-Computer)
C. Category III - Peripheral to Peripheral (Inter-Peripheral)
2.2.3  PARALLEL INTERFACE CATEGORY CONFIGURATION

In Category II mode the Output port operates as a Peripheral device and the Input port operates as a Computer. In Category III mode the Output port operates as a Computer and the Input port operates as a Peripheral device. In the Passive Monitor mode the Output port is placed in the tristate mode and the Input port records the transfers between two other NTDS devices. Additionally, the Computer interfaces can be configured to operate with either interlocked or pulsed signal timing.

2.2.4  PARALLEL INTERFACE TIMING

The state ( logic 1 or 0 ) of the NTDS Data lines is determined by their DC voltage level, and do not have to be cleared between successive transactions. The only restriction is that the Data lines must be stable during that time that the associated control line indicates validity. The control signals are edge significant and the receiving device must be able to recognize their change of state ( from logic 1 to 0 or 0 to 1 ). The receiving device must not recognize a subsequent logic 1 until that line first transitions to the logic 0 state.

2.2.5  PARALLEL INTERFACE TYPES

Parallel interface channels can be configured to operate in NTDS TYPE A ( SLOW ), TYPE B ( FAST ), TYPE C ( ANEW ), or TYPE H ( HIGH THROUGHPUT ) environments. A special TRISTATE ( OPEN CABLE ) mode is also provided. Figure 2.1 illustrates the required electrical connection schemes for each type.

2.2.5.1  TYPE A ( SLOW )

The Type A mode, also called SLOW, supports transfer rates of 41.67 K words per second on one cable. Nominal voltage levels of 0.0 VDC ( logic 1 ), -15 VDC ( logic 0 ), and switching thresholds of -6 VDC are used. Controlled slew rate driver outputs with linear characteristics are required. The single ended receiver circuits must be able to reject input transient pulse signals with specific maximum energy levels ( 30 Vµs ). The receiver outputs must be logic 0 for open input conditions. Maximum specified cable lengths are 300 ft.

2.2.5.2  TYPE B ( FAST )

In Type B mode, also called FAST, transfer rates of 250 K words per second on one cable are possible. Nominal voltage levels of 0.0 VDC ( logic 1 ), -3 VDC ( logic 0 ), and switching thresholds of -1.5 VDC are used. The referenced input receiver circuits must reject large common mode input transient pulses or DC signals ( +/- 7.5 VDC ). The receiver outputs must be logic 0 for all open input conditions. Controlled slew rate driver outputs are required. Depending on cable type used, maximum specified cable lengths are 50 or 100 ft.

2.2.5.3  TYPE C ( ANEW )

The Type C mode, also called ANEW, supports transfer rates of 250 K words per second on one cable. Nominal voltage levels of 0.0 VDC ( logic 1 ), +3.5 VDC ( logic 0 ), and thresholds of +1.5 VDC are used. The referenced input receivers must reject large common mode input transient pulses or DC signals ( +/-6 VDC ). The receiver outputs must be logic 0 for all open input conditions. Controlled slew rate driver outputs are required. Depending on cable type used, maximum specified cable lengths are 100 or 250 ft.
2.2.5.4 TYPE H (HIGH THROUGHPUT)

In Type H mode, also called HIGH THROUGHPUT or FAST ANEW, transfer rates of 500 K words per second on one cable are possible. Nominal voltage levels of 0.0 VDC (logic 1), +3.5 VDC (logic 0), and thresholds of +1.5 VDC are used. The referenced input receivers must reject common mode input transient pulse or DC signals (+/- 6 VDC). The receiver outputs must be logic 0 for all open input conditions. Controlled slew rate driver outputs are required. Depending on cable type used, maximum specified cable lengths are 100 or 250 ft.

2.2.5.5 DRIVER TRISTATE (OPEN CABLE)

To allow for bussed configurations, hot spares, connection errors, and other unanticipated connection configurations, while the tristate mode is selected the NTDS outputs shall not be damaged nor shall they present less than 100,000 ohms impedance when they are driven by an externally connected signal source. When the tristate mode is selected the NTDS outputs will not be damaged by voltage excursions that are within the range of plus 10 volts to minus 18 volts with respect to the driver signal return connection.

2.2.5.6 ADDITIONAL RECEIVER CHARACTERISTICS

The NTDS inputs shall not be damaged by voltage excursions that are in the range of 15 VDC to minus 24 VDC, with respect to the signal return connection. When the inputs are driven beyond the maximum operating limits they may temporarily sink or source more current than specified. The output of the receiver shall not switch as a result of any input signal that has an amplitude between plus 7.5 VDC to minus 17.5 VDC if the duration and amplitude are common to the input and the return connection (common mode).

2.3 CATEGORY I OUTPUT PORT OPERATION

Transfer of information between NTDS computers and peripherals is accomplished using two methods: Data and Functions. The Output Port transactions are controlled by the Peripheral's request lines and the Computer's acknowledge lines.

2.3.1 OUTPUT DATA TIMING

A peripheral device sets its Output Data Request (ODR) line when it is in a condition to accept an Output Data (OD) word from the NTDS computer. The computer responds, at its convenience, by activating its Output Data Acknowledge (ODA) line. The active ODA line indicates to the peripheral device that the data contained on the OD lines is valid and should be sampled. The peripheral device acknowledges the receipt of data by deactivating its ODR line. The signal timing relationships for Output Data transfers are shown in Figure 2.3.

2.3.2 EXTERNAL FUNCTION TIMING

A peripheral device sets its External Function Request (EFR) line when it is in a condition to accept an External Function (EF) command word from the NTDS computer. The computer responds, at its convenience, by activating its External Function Acknowledge (EFA) line. The active EFA line indicates to the peripheral device that the command word contained on the OD lines is valid and should be sampled. The peripheral device acknowledges the receipt of data by deactivating its EFR line. Figure 2.4 illustrates External Function timing.
2.3.2.1 FORCED EXTERNAL FUNCTION TIMING

Some NTDS computers have the ability of sending External Functions with Force. These transfers require no request (EFR) from the peripheral device. The computer, at its convenience, activates its External Function Acknowledge (EFA) line, indicating to the peripheral device that the command word contained on the OD lines is valid and should be sampled. The EFR line is not monitored during the Forced EF. The peripheral device has no control over the rate at which Forced EFs are sent.

2.4 CATEGORY I INPUT PORT OPERATION

Transfer of information between NTDS computers and peripherals is accomplished in two major methods: Data and Interrupts. The Input Port transactions are controlled by the Peripheral's request lines and the Computer's Input Acknowledge and Interrupt Enable lines. Only one of the peripheral's request lines line may be active at any one time.

2.4.1 INPUT DATA TIMING

An active Input Data Request (IDR) indicates to the computer that the peripheral has placed valid data on the data lines. The Computer's Input Data Acknowledge (IDA) line indicates to the peripheral that it has sampled this data. When the peripheral device senses that the IDA line is active it deactivates its IDR line. When the computer deactivates its IDA line the input cycle is complete. Figure 2.5 illustrates Input Port control signal timing.

2.4.2 EXTERNAL INTERRUPT TIMING

Transmission of External Interrupt words from the peripheral device to the computer is controlled by the External Interrupt Enable (EIE) line. When sending an External Interrupt the peripheral activates its External Interrupt Request (EIR) line indicating the validity of the interrupt data on the data lines. At its convenience the computer accepts the interrupt code, deactivates its EIE line and activates its IDA line. The peripheral device senses that the IDA line is active and responds by deactivating its EIR line. When the computer deactivates its IDA line the input cycle is complete. That not all computers have an EIE line and peripheral equipment may be designed to initiate an External Interrupt transfer without monitoring the EIE line. This does not, however, alter the timing sequence since the computer will still accept the interrupt at its own convenience using the IDA line. Refer to Figure 2.6.

2.5 NTDS CHANNEL IMPLEMENTATION

The MIL-STD-1397C (NAVY) Specification allows a wide variation in the implementation of NTDS channel interface design architectures. This allows the designer to develop circuits which maximize total system channel throughput. The GET NTDS channels are designed to take full advantage of these modes. The three main design schemes currently used are:

A. Interlocked
B. Pipeline
C. Pulse
2.5.1  INTERLOCKED OPERATION

In Interlocked timing, the most fundamental transaction protocol, the peripheral device will not initiate a subsequent transaction until the current transaction has completely finished. The NTDS timing specifications still allow the channel to operate at full transfer rates as long as the peripheral device does not extend any active request lines beyond the minimum required time.

2.5.1.1  INTERLOCKED OUTPUT TIMING

A peripheral device sets its Request (ODR or EFR) lines when it is in a condition to accept an Output from the computer. The computer responds, at its convenience, by activating its Output Acknowledge line (ODA or EFA), indicating that the data is valid. The peripheral then samples the data and may deactivate its Request line any time after that. The computer maintains its acknowledge line active until the minimum pulse width period has expired or, if the peripheral device has not yet deactivated the Request line, until the request line is deactivated (whichever comes last). The Output cycle is completed when the computer deactivates its acknowledge line. Figures 2.3 and 2.4 illustrate the Output Port signal timing.

2.5.1.2  INTERLOCKED INPUT TIMING

When the peripheral device wishes to send information to the computer it places the associated data on the data lines and activates an Input Request (IDR or EIR). The computer samples the data lines and activates the Input Data Acknowledge (IDA). The peripheral device may deactivate its request line at any time after sensing that the IDA line has been activated. The computer continues to maintain its IDA line active until the minimum pulse width time has expired or, if the peripheral device has not yet deactivated the Input Request line, until the request line is deactivated (whichever comes last). When the computer deactivates its IDA line the input cycle is considered completed. Figures 2.5 and 2.6 illustrate the port Input control signal timing.

2.5.2  PIPELINE OPERATION

Pipelined timing (Figure 2.7) enables a channel to operate at maximum transfer rates by allowing the peripheral device to request the next transfer during the closing phase of the current transaction. This is possible because the request minimum low time can then be satisfied during the acknowledge minimum pulse width times, and then reactivated, requesting the next transfer before the initial acknowledge pulse period has expired. This feature allows the cable control line propagation delays to occur during the acknowledge pulse width and hold times, where they do not affect total system throughput.

2.5.2.1  PIPELINED OUTPUT TIMING

A peripheral device sets its Request (ODR or EFR) lines when it is ready to accept an Output. At its convenience, the computer responds by presenting valid data and activating the appropriate acknowledge line (ODA or EFA). The peripheral samples the data, deactivates its Request line, and starts a Request line inactive timer. The computer continues to maintain its acknowledge line active until its minimum pulse width time has expired. The peripheral device, after the minimum low time has been satisfied, reactivates the Request line, regardless of the state of the computer acknowledge line. When the computer deactivates its acknowledge line the current output cycle is complete, and if the request line has been reactivated, a new cycle can begin immediately.
2.5.2.2 PIPELINED INPUT TIMING

When the peripheral wishes to send information to the computer it places valid data on the data lines and activates an Input Request ( IDR or EIR ). The computer samples the data lines and activates the Input Data Acknowledge ( IDA ). When the peripheral device senses that the IDA line is active may deactivate its Request line, and start a Request line inactive timer. The computer continues to maintain its IDA line active until the minimum pulse width time has expired. The peripheral device, after its minimum low time has been satisfied, may present a new data word and reactivate the Input Request line, regardless of the state of the computer IDA line. When the computer deactivates its IDA line the current input cycle is complete, and if the request line has been reactivated, a new cycle can begin.

2.5.3 PULSED OPERATION

The pulsed operation can be used for both the interlocked and pipelined modes. In pulsed operation computer is designed to maintain its active acknowledge lines for only the minimum required period, regardless of the state of the corresponding peripheral request lines. Pulsed mode timing is illustrated in Figure 2.8.

2.5.3.1 PULSED OUTPUT TIMING

A peripheral device sets its Request ( ODR or EFR ) lines when it is in a condition to accept an Output from the NTDS computer. The computer responds by activating its Output Acknowledge line and maintaining it active until its minimum pulse width time has expired. The computer then deactivates the acknowledge line, regardless of the state of the request line. The peripheral device may deactivate its Request line at any time after the acknowledge line has been activated. The peripheral device can reactivate the Request line and start the next cycle only after its request line minimum low time.

2.5.3.2 PULSED INPUT TIMING

When the peripheral wishes to send information to the computer it activates an Input Request line ( IDR or EIR ). The computer samples the data lines and activates the Input Data Acknowledge ( IDA ), which remains active until the minimum pulse width time has expired. The computer then deactivates the acknowledge line, regardless of the state of the request line. The peripheral device may deactivate its Request line at any time after the IDA line has been activated. The peripheral device can reactivate the Request line and start the next cycle only after its request line minimum low time requirement has been met.
FIGURE 2.1
ELECTRICAL CONNECTIONS

FIGURE 2.2
NTDS CHANNEL CONNECTIONS
FIGURE 2.3
OUTPUT DATA TIMING

FIGURE 2.4
EXTERNAL FUNCTION TIMING
FIGURE 2.5

INPUT DATA TIMING

FIGURE 2.6

EXTERNAL INTERRUPT TIMING
FIGURE 2.7
PIPELINE MODE TIMING

FIGURE 2.8
PULSED TIMING EXAMPLE
3.1 NTDS TYPE D SERIAL

The following discussion addresses the general design philosophy used in the design of GET NTDS Type D Serial Interface adaptors and supporting products. This discussion is intended as an aid in explaining a general operation of an NTDS Type D channel and does not cover all protocol aspects. For a complete protocol description refer to MIL-STD-1397C (NAVY) Military Standard Document.

3.1.1 NTDS TYPE D SERIAL OVERVIEW

The GET NTDS Type D Serial Interface Adaptors transfer 10 Mb/s binary information using bipolar serial pulse trains on two coaxial cables. An NTDS Type D I/O CHANNEL consists of a Input (Sink) Port and a Output (Source) Port, each of which can transact a 34 bit information frame using two types of 3 bit control frames. The signals required for an input transaction occur entirely on the single coaxial cable used for the Input Port. The signals required for an output transaction occur entirely on the single coaxial cable used for the Output Port.

3.2 NTDS TYPE D SERIAL TRANSACTIONS

Information transfers between two devices is accomplished using 10 Mb/s control and data frame bipolar pulse trains. The transmitting device sends a control frame requesting an eventual word transfer to the receiving equipment. The receiving equipment then sends a control frame granting or denying permission to the requesting device to transmit the data frame. If the transmission request is denied the transmitting device may elect to send another output request control frame. If the control frame indicates that permission has been granted the transmitting device sends the data frame.

3.3 NTDS TYPE D SERIAL TIMING

The encoding scheme used is called Manchester Encoding. In this scheme the transmission clock and data are encoded into each bit. This 10 Mb/s timing has a 100 nanosecond period for each bit time. Each bit time is in turn divided into two 50 nanosecond pulse periods. A logical 1 is represented by a positive pulse followed by a negative pulse. A logical 0 is a negative pulse followed by a positive pulse.

3.3.1 TYPE D INTERFACE VOLTAGES

At the transmitter end of the coaxial cable the serial data line has an amplitude of +/- 3.25 Volts. The switching threshold at the receiver end of the coaxial cable is +/- 1.25 VDC. Additionally, the receiver outputs must remain stable and not switch state for all open input conditions or when the input voltage is between 0.00 and +/- 0.5 VDC. With RG-12A coaxial cable and 75 Ohm termination the maximum specified cable length is 1000 ft (Figure 3.2).
3.3.2 CONTROL FRAME FORMAT

The first bit of each three bit control frame (Figure 3.1) pulse train is a logic 1 synchronization bit. The next two bits represent the Data and Function requests and enables. Both bits may be set in any control frame. A data or function word can be transmitted following a control frame exchange.

3.3.3 DATA FRAME FORMAT

The first bit of each thirty four bit data frame pulse train is a logic 1 synchronization bit. The next bit is the word identifier (0 for Data and 1 for Functions/Interrupts). The next 32 bits represent the transmitted data. No parity or other check bits are specified (Figure 3.2).

3.4 SERIAL INTERFACE CATEGORIES

The NTDS Type D Serial interface channels are specified to operate as Computer or Peripheral channels in order to support the three NTDS equipment categories defined in MIL-STD-1397C. These equipment categories are:

A. Category I - Computer to Peripheral
B. Category II - Computer to Computer (Inter-Computer)
C. Category III - Peripheral to Peripheral (Inter-Peripheral)

3.4.1 CATEGORY I OUTPUT OPERATION

In Category I Computer Output operation the Computer Output Channel is connected to a Peripheral Input Channel. The Computer transmits Output Enable Control Frames (OECF) with the Output Data Enable (ODE) and External Function Enable (EFE) bits indicating its readiness to transmit. The Peripheral device's Input Channel transmits Output Request Control Frames (ORCF) with the Output Data Request (ODR) and External Function Request (EFR) bits indicating its ability to receive. The actual data frame transaction follows the sequence described in Paragraph 3.5.

3.4.2 CATEGORY I INPUT OPERATION

In Category I Computer Input operation the Computer Input Channel is connected to a Peripheral Output Channel. The Peripheral transmits Input Request Control Frames (IRCF) with the Input Data Request (IDR) and External Interrupt Request (EIR) bits indicating its readiness to transmit. The Computer device's Input Channel transmits Input Enable Control Frames (IECF) with the Input Data Enable (IDE) and External Interrupt Enable (EIE) bits indicating its ability to receive (refer to Paragraph 3.5).

3.4.3 CATEGORY II OPERATION

In Category II operation the Computer Output Channel is connected to a Computer Input Channel. The transmitting Computer sends an OECF with the ODE and EFE bits indicating its readiness to transmit. The receiving Computer Input Channel interprets the OECF as an IRCF, with the ODE as the IDR and the EFE as the EIR. The receiving Computer Input Channel transmits an IECF with the IDE and EIE bits indicating its ability to receive. The transmitting Computer Output Channel interprets the IECF as an ORCF, with the IDE as the ODR and the EIE as the EFR (refer to Paragraph 3.5).
3.4.4 CATEGORY III OPERATION

In Category III operation the Peripheral Output Channel is connected to a Peripheral Input Channel. The transmitting Peripheral transmits an IRCF with the IDR and EIR bits indicating its readiness to transmit. The receiving Peripheral Input Channel interprets the IRCF as an OECF, with the IDR as the ODE and the EIR as the EFE. The receiving Peripheral Input Channel transmits an ORCF with the ODR and EFR bits indicating its ability to receive. The transmitting Peripheral Output Channel interprets the ORCF as an IECF, with the ODR as the IDE and the EFR as the EFE. The actual data frame transaction follows the sequence described in Paragraph 3.5.

3.5 SERIAL TRANSFERS

When viewed on a bit by bit basis, the data frame transaction operations between Computer and Peripheral devices is essentially the same regardless of Category. The main difference is in the control frame and bit naming conventions used. In short, the transmitter to receiver link works the same for all three categories, with the similar timing and event sequences. Therefore, only the Category 1, Computer Output to Peripheral Input transaction, will be described in detail in the following paragraphs. The transmitting device sends a control frame requesting that the receiving device accept it. The receiving device responds with a control frame indicating its ability to accept the data frame. The transmitting device, in accordance with internal priorities, sends another control frame or sends the data frame.

3.5.1 DATA FRAME TRANSFERS

Transfers of information between NTDS Input and Output devices are accomplished in two major methods: Data and Functions. An OUTPUT device sets the Output Data Enable (ODE) bit or External Function Enable (EFE) bit when it is in a condition to transmit a Data or External Function word to the INPUT device. The OUTPUT device then sends an Output Enable Control Frame (OECF) with the ODE or EFE bits (or both) set. The INPUT device responds by transmitting an Output Request Control Frame (ORCF). The ORCF indicates the INPUT Channel's ability to accept the data frame offered by the OUTPUT device, as determined by the condition of the Output Data Request (ODR) or External Function Request (EFR) bits. The active request bit indicates to the OUTPUT device that the INPUT device can accept the requested transfer. The OUTPUT device, at its convenience, sends the OD or EF data frame to the INPUT device. Note that both ODE and EFE bits may be active at any one time. The INPUT device acknowledges the receipt of data frame and its ability to accept another data frame by transmitting another ORCF frame. Figures 3.1 and 3.2 illustrate the TYPE D control and data frame formats.

3.5.2 FORCED EXTERNAL FUNCTIONS

Some NTDS computers have the ability of sending External Functions with Force and do not require that the EFR bit be set in the Input device’s ORCF. The INPUT device has no control over the rate at which External Functions with Force are sent. If the INPUT device can not accept External Functions at a high rate, timing restrictions must be made in the computer programming or external data rate buffering devices may have to be used. The typical GET TYPE D interface contains an input FIFO structure that can accept several consecutive Forced External Functions before the danger of lost data arises.
FIGURE 3.1
CONTROL FRAME TIMING

FIGURE 3.2
DATA FRAME TIMING
SECTION 4
NTDS TYPE E SERIAL INTERFACE

4.1 NTDS TYPE E SERIAL

The following discussion addresses the general design philosophy used in the design of GET NTDS Type E Serial Interface adaptors and supporting products. This discussion is intended as an aid in explaining a general operation of an NTDS Type E channel and does not cover all protocol aspects. For a complete protocol description refer to MIL-STD-1397C (NAVY) Military Standard Document.

4.1.1 NTDS TYPE E SERIAL OVERVIEW

The GET NTDS Type E Serial (LLS) Interface Adaptors transfer 10 Mb/s binary information using bipolar serial pulse trains on two triaxial cables. A LLS I/O CHANNEL consists of a Source (Output) Port and a Sink (Input) Port each of which can transact information frames using two types of 4 bit control frames. The signals required for an input transaction occur entirely on the single triaxial cable used for the Sink Port. The signals required for an output transaction occur on the single triaxial cable used for the Source Port.

4.2 NTDS TYPE E SERIAL TRANSACTIONS

Transfers of information between two serial devices is accomplished using 10 Mb/s control and data frame bipolar pulse trains. The transmitting device sends a control frame requesting an eventual word transfer to the receiving equipment. The receiving equipment then sends a control frame granting or denying permission to the requesting device to transmit the data frame. If the transmission request is denied the transmitting device may elect to send another output request control frame. If the control frame indicates that permission has been granted the transmitting device sends the data frame.

4.3 NTDS TYPE E SERIAL TIMING

The encoding scheme used is called Manchester II Split Phase Encoding. In this scheme the transmission clock and data are encoded into each bit. This 10 Mb/s timing has a 100 nanosecond period for each bit time. Each bit time is in turn divided into two 50 nanosecond pulse periods. A logical 1 is represented by a positive pulse followed by a negative pulse. A logical 0 is a negative pulse followed by a positive pulse.

4.3.1 TYPE E INTERFACE VOLTAGES

At the transmitter end of the coaxial cable the serial data line has an amplitude of +/- 0.600 Volts. The switching threshold at the receiver end of the coaxial cable is +/- 0.220 VDC. Additionally, the receiver outputs must remain stable and not switch state for all open input conditions or when the input voltage is between 0.00 and +/- 0.155 VDC. The receiver input circuits must also be able to reject input transient pulses of specific energy levels. With MIL-C-17/134 triaxial cable and 50 Ohm termination the maximum specified cable length is 390 ft. With MIL-C-17/135 triaxial cable and 50 Ohm termination the maximum specified cable length is 980 ft (Figure 4.1).
4.3.2 CONTROL FRAME FORMAT

There are two types of control frames used in the LLS transaction protocol (Figure 4.2). The Source Status Control Frame (SOS) is used by the Source device to indicate its readiness to transmit Information Frames. The Sink device uses the Sink Status Control Frames (SIS) to indicate its readiness to receive. The first bit of these four bit control frames is a logic 1 synchronization bit. The next two bits represent the Data and Function requests and enables. Both bits may be set in any control frame. The fourth control frame bit is the control frame identifier bit (ID). The polarity of the ID bit is user selectable on GET interface adaptors.

4.3.3 INFORMATION FRAME FORMATS

The information frame transmitted as a result of the control frame exchange is identified by the information word identifier bit (Figure 4.3). There are two types of Information Frames (IF) used. The Single Word Transfer (SWT) Frames transfer single 34 or 35 bit Data or Command/Interrupt (CIW) words. The Burst transfer frame is used to send up to 32 Data words in a single transaction. The first bit of each IF is a logic 1 synchronization bit. The next bit is the word identifier (WI, 0 for Data and 1 for CIW). The next 32 bits represent the transmitted data, followed by an optional ODD parity bit. For burst frames, up to 31 additional Data words, with optional parity, follow. CIWs can not be sent as Burst frames.

4.4 SERIAL TRANSFERS

A SOURCE device sets its Output Data Enable (ODA) line or External Function Enable (EFA) line when it is in a condition to transmit a Data or CIW word to the SINK device. The SOURCE device then sends a SOS frame with the ODA or EFA bits set. The SINK device responds to the SOS by transmitting a SIS frame. The SIS indicates the SINK port's ability to accept the data frame offered by the SOURCE device with the Output Data Request (ODR) and External Function Request (EFR) bits. The active request bit indicates to the source device that the SINK device can accept the requested transfer. Note that both ODR and EFR bits may be active at any one time. The SOURCE device, at its convenience and according to internal priorities, sends the SWT or Burst IF to the SINK device. The SINK device acknowledges the receipt of data and its possible ability to accept another IF by sending another SIS frame.

4.4.1 FORCED EXTERNAL FUNCTIONS

Some NTDS devices have the ability of sending a Forced CIW and do not require that the EFR bit be set in the SIS frame. The SINK device has no control over the rate at which CIWs with Force are sent. If the SINK device can not accept the CIWs at a high rate, timing restrictions must be made in the computer programming or external data rate buffered devices may have to be used. The GET interface adaptors contain input FIFO buffers that can accept several consecutive Forced CIWs before the danger of lost data arises.
4.5 SYSTEM INTEGRITY FEATURES

The LLS System Integrity Features (SIF) are designed to improve system reliability. Using SIF, the user can determine if an LLS interface is improperly connected, disabled, or malfunctioning. The SIF error detection logic is designed to detect communications loss, protocol violations, and data corruption. The SIF monitors are designed to operate simultaneously and without interfering with normal LLS protocol operations. The monitored error conditions include Sink and Source port CF timeouts, IF parity, CF validation, CF and IF framing errors, and CF and IF response errors. No corrective action is specified if a SIF error is detected. However, when a SIF error condition is detected the operator must be notified by appropriate register settings or, if implemented, a status indicator.

FIGURE 4.1
LLS ELECTRICAL CONNECTIONS
FIGURE 4.2
LLS CONTROL FRAME TIMING

FIGURE 4.3
LLS DATA FRAME TIMING
SECTION 5
GET NTDS INTERFACE ADAPTORS
KEY OPERATIONAL FEATURES

5.1 GENERAL ORGANIZATION

The GET NTDS interface adaptors are divided into three major functional
modules including the NTDS Input Port, NTDS Output Port, and the local host Bus
Interface and controller (Figure 5.1). The structure and operation of the
NTDS ports is identical for all interface types and the functional descriptions
provided apply to all GET NTDS interface adaptors.

5.2 NTDS INPUT PORT

The NTDS Input Port (serial SINK) accepts data from the attached device
and consists of the Input Register, the Input FIFO, and the Extract Register.
Transaction timers monitor the operation of the Input and Extract ports and
alert the system software when a command or transaction timeout condition
exists. From the perspective of the externally connected NTDS device the Input
and Extract Registers form a single NTDS Input Port. The Input Register data
path is intended for use for large volume transactions and is connected to a DMA
controller. The Input FIFO provides the ability to transact and buffer the NTDS
data without compromising the system bus bandwidth. The Extract Register is
intended for single word transactions and is serviced directly by the system
processor. The Input and Extract Registers operate independently and both may
be active at any one time.

5.2.1 INPUT PORT DATA PATH

Received NTDS data is transferred from the Input Port to system memory
using the Input Register DMA or Extract Port facilities. The Input Data
initially passes through the Input Data Receivers to the Input FIFO or to the
Extract Register. The Input FIFO architecture provides automatic sorting of
Input Data and other requested transactions (Terminating transactions and
Forced Functions) while maintaining timing coherency. The Input FIFO also
serves as a caching rate buffer which allows NTDS Input Data to be received at
the highest allowable rate, regardless of system bus capacity. The DMA
controller and FIFO also serve as a rate buffer that allows the NTDS data to be
assembled and transferred to memory at the maximum allowable system bus rate.
The Extract path data consists of a single 32 bit register which is directly
accessed by the system processor.

5.3 NTDS OUTPUT PORT

The NTDS Output Port (serial SOURCE) sends data to the attached device
and consists of the Output Register and the Insert Register. From the
perspective of the externally connected NTDS device the Output and Insert
Registers form a single NTDS Output Port. The Output Register is intended for
use for large volume transactions and is connected to the DMA controller. The
DMA FIFO provides the ability to assemble and buffer the NTDS data without
compromising the system bus bandwidth. The Insert Register supports single word
transactions and must be directly serviced by the system processor. The Output
and Insert Registers operate independently and may be simultaneously active.
5.3.1 OUTPUT PORT DATA PATH

Data is transferred from system memory to the Output Port using DMA or Insert Port facilities. The DMA transfers pass through the system bus interface to the Output Register and then to the Output Data Drivers, which hold the actual NTDS data being transacted. The Insert path data consists of a single 32 bit Insert Data Register which is directly accessed by the system processor.

5.4 PROTOCOL OPERATIONS

Modern communication protocols generally consist of a set of Request and Acknowledge transactions to negotiate the transfer of blocks of data. A typical example of this process is illustrated in Figure 5.3 (A & B). All GET interface adaptors support Half Duplex and Full Duplex protocol operations. Full duplex protocol operations are possible because all Input Port and Output Port components are independent and may be active at any time.

5.4.1 HALF DUPLEX OPERATIONS

Half Duplex channels are generally found on peripheral devices like tape drives, display systems, and printers. In these systems all operations are CPU initiated and data buffers are transferred in only one direction at a time. In other words either the input buffer or the output buffer may be active at one time. The protocol normally consists of an EF command code word followed by the required OD or ID. At the end of the command the peripheral device may issue a status EI code word (Figure 5.2). Data and command coherency (the order in which OD/ID and EF/EI are transferred) are very important in these systems as the EF/EI transfers are generally used to bound the OD/ID buffers.

5.4.1.1 HALF DUPLEX SUPPORT

Half Duplex protocol operations with built in data and command coherency are easily performed using the Output and Input Ports. Output Commands (Figure 5.2A) can be transmitted using the Split Buffer Output feature. This operation will transmit an EF followed by the OD buffer. Command completion can be specified to be the end of buffer, interword timeout, or Buffer/Command timeout. The received EI status word can then be read out using the Read Function command. Input Commands (Figure 5.2B) are transmitted using the Output Function feature and the required ID can be received using the Receive Data with Abort on Function feature. This operation will transmit an EF followed by the opening of an ID buffer. Command completion can be specified to be the end of buffer, reception of the EI status word, interword timeout, or Buffer/Command timeout. The received EI word can be read out using the Read Function command.

5.4.2 FULL DUPLEX OPERATIONS

Full Duplex operations are generally used on inter-computer channels and intelligent peripheral devices like navigation systems and data processors. In these systems either device may independently initiate a data transfer and the input and output buffers may both be active simultaneously. The protocol normally consists of an EF and EI exchange to negotiate the buffer transfer followed by the required OD or ID buffer. The transmitting device may optionally send an end of command EI status word. Data and command coherency are less important in these systems as the EF/EI code words are used to enable the data buffers rather than to bound them (Figure 5.3).
5.4.2.1 FULL DUPLEX SUPPORT

Full Duplex protocol operations are performed on GET interface adaptors using the single word Insert and Extract ports for the EF/EI operations and the Output and Input Ports for the OD/ID buffers. Command completion can be specified to be the end of buffer, interword timeout, or Buffer/Command timeout.

5.5 INTERVAL TIMERS

The Input and Output ports each contain a set of interval timers that are used as a Command or Buffer timer and an interword timer (Figure 5.4). The Insert and Extract registers only have Command timers. These timers have 1 microsecond clocking granularity and automatic stop/start controls. These timers are automatically disabled at buffer completion.

5.5.1 TRANSACTION QUALITY TIMING

Most tactical devices have specified command response times and data transfer rates that must be met in order to be considered fully operational. As an interface quality control mechanism, timeouts can be used to indirectly indicate the operational status of these devices. Limit values for the Buffer and Interword timers can be calculated using the specified response times, transfer rates, and buffer size information.

5.5.2 COMMAND/BUFFER TIMEOUT TIMER

The Command/Buffer Timeout Timer generates an interrupt signal when the timer expires. The timer is initialized by loading a value representing the desired timeout period. Values from 1 microsecond to 36 minutes can be used. When the Command Timeout Mode is selected the timer countdown starts when the command is started. When the Buffer Timeout Mode is selected and the timer countdown starts on the initial SET to CLEAR transition of the data ready status bit (indicating that the first word of the buffer has been transacted).

5.5.3 INTERWORD TIMEOUT TIMER

The Interword Timeout Timer generates an interrupt when the specified time between NTDS transactions is exceeded. Timeout values from 1 microsecond to 65 seconds can be used. The timer countdown starts on the initial SET to CLEAR transition of the data ready status bit (indicating that the first word of the buffer has been transacted). The timer is automatically reinitialized each time the data ready status is set.

5.5.3.1 END OF BUFFER TIMEOUT

The Interword Timeout Timer can be used to determine actual buffer size in systems (such as tape drives) which have variable or undetermined buffer sizes. An Input or Output command with a buffer size larger than the maximum expected can be started. If a timeout value larger than the maximum expected time between data transfers is specified, an Interword Timeout interrupt will be generated when the device stops transacting data (the end of it’s buffer). This timeout can be interpreted as the end of buffer signal.
FIGURE 5.1

INTERFACE CONFIGURATION

FIGURE 5.2

HALF DUPLEX OPERATION

FIGURE A: TYPICAL OUTPUT DATA BUFFER TRANSFER

FIGURE B: TYPICAL INPUT DATA BUFFER TRANSFER
FIGURE 5.3
FULL DUPLEX OPERATION

FIGURE 5.4
TRANSACTION TIMEOUT OPERATION
SECTION 6
ATDS SERIAL INTERFACE

6.1 ATDS SERIAL OVERVIEW

The following discussion is a brief operational description of a typical ATDS serial channel. It is intended as an aid in explaining the operation of this link and as such does not cover all aspects of the ATDS communication protocol. Refer to MIL-STD-188-203-1A (Appendix D2) Military Standard Document for a complete description of ATDS data exchange protocols.

6.2 SERIAL TRANSFERS

Transfers of information between ATDS Data Terminal Sets (DTS) and Tactical Data System (TDS) Computers are accomplished on a single cable in a complex half duplex mode (Figure 6.4). Three transfer operations are used: DTS to TDS data, TDS to DTS data, and TDS to DTS Address transfers.

6.2.1 DTS TO TDS DATA TRANSFERS

Data transfers from the DTS to the TDS computer are performed using the Frame, Data Clock, Incoming Data, and Outgoing Data Lines (Figure 6.1). The DTS generates a pulse on the Frame line when it desires to transmit a data frame to the TDS computer. When the computer is ready to receive, it issues a series of 26 pulses on the Data Clock Line to shift the serial data on the Incoming Data Line from the DTS to the computer. After a minimum delay of 7 microseconds the computer generates a second series of 26 clock pulses which resends the same serial data from the DTS to the computer again. The computer then compares the two received data words and, if they are not identical, generates a fault pulse on the Outgoing Data Line.

6.2.2 TDS TO DTS DATA TRANSFERS

Data transfers from the TDS computer to the DTS are performed using the Frame, Data Clock, Incoming Data, and Outgoing Data Lines (Figure 6.2). The DTS generates a pulse on the Frame line when it desires to receive a data frame from the TDS computer. When the computer is ready to transmit, it issues a series of 26 pulses on the Data Clock Line to shift the serial data on the Outgoing Data Line from the computer to the DTS. After a minimum delay of 7 microseconds the computer generates a second series of 26 clock pulses which returns the serial data just received from the computer back to the computer. The computer then compares the two received data words and, if they are not identical, generates a fault pulse on the Outgoing Data Line.

6.2.3 TDS TO DTS ADDRESS TRANSFERS

Address Frame transfers from the Tactical Data System computer to the DTS are performed using the Frame, Incoming Data, and Address Data, and Address Clock Lines (Figure 6.3). When the DTS desires to receive an address frame from the TDS computer it generates a simultaneous pulse on the Frame and Incoming Data lines. When the computer is ready to transmit, it issues a series of 7 pulses on the Address Clock Line to shift the serial data on the Address Data Line from the computer to the DTS.
6.2.4 DTS TO TDS DATA FORMAT

The 26 bit DTS to TDS serial data frame consists of two leading Control Bits (C1 and C2) followed by 24 Data Bits. The Control bits are used to indicate the quality of the received data. Control Bit C1 is generally used to indicate the presence of detected errors in the data field. Control Bit C2 is used as the frame start indication. This bit is SET in the first frame and CLEAR for all subsequent frames of each message.

6.2.5 DTS TO TDS ADDRESS FORMAT

The 7 bit DTS to TDS serial address frame consists of 6 leading Address Bits followed by a single Message Control Bit. The Message Control bit is typically used to define the message format to be used by the DTS during transmission.

6.2.6 TDS TO DTS DATA FORMAT

The 26 bit TDS to DTS serial data frame consists of two leading Control Bits (C1 and C2) followed by 24 Data Bits. The Control bits are used to indicate the type of the transmitted data. The data frame is valid when Control Bits C1 and C2 are both SET. A stop condition is indicated when either C1 or C2 are CLEAR. In this case the DTS will typically discard the data portion of the frame and transmit a special stop code.

6.3 SIDETONE INTERFACE OPERATION

The Sidetone Frame, Sidetone Data, and Sidetone Clock lines are used for test and data validation purposes. The Sidetone Interface provides an additional echo data path that returns to the TDS computer the data that was transmitted by the DTS.

6.3.1 DTS TO TDS SIDETONE TRANSFER

The 26 bit TDS to DTS serial data frame consists of two leading Control Bits followed by 24 Data Bits. The Sidetone transfers from the DTS to the TDS computer are performed using the Sidetone Frame, Sidetone Data, and Sidetone Data Clock (Figure 6.3). The DTS generates a pulse on the Sidetone Frame line when it desires to transmit a Sidetone Data frame to the TDS computer. When the computer is ready to receive, it issues a series of 26 pulses on the Sidetone Clock Line to shift the serial data on the Sidetone Data Line from the DTS to the computer. The computer then uses the received Sidetone Data to evaluate the transmission performance of the DTS.

6.4 ELECTRICAL CHARACTERISTICS

The signal interface lines between the TDS computer and the DTS are measured across a 100 Ohm load on the secondary winding of a terminating transformer. The amplitude of all pulses is -6 VDC, with respect to ground. This voltage is 0.0 VDC when no pulses are present. The width of the pulses from the TDS to the DTS is 200 nanosec. The width of the pulses from the DTS to the TDS is 600 nanosec. The nontactical interface (sidetone) lines have open collector drivers with the capability of sinking 20 mA to ground. The amplitude of the sidetone signals is nominally +5 VDC, with respect to ground. The sidetone receiver switching threshold is 1.5 VDC.
FIGURE 6.1
DTS TO TDS DATA FRAME TIMING

FIGURE 6.2
TDS TO DTS DATA FRAME TIMING
FIGURE 6.3
SIDETONE AND ADDRESS FRAME TIMING

FIGURE 6.4
ATDS ELECTRICAL CONNECTIONS
SECTION 7  
PASSIVE TAP MONITOR

7.1 GENERAL PRODUCT DESCRIPTION

All GET Engineering NTDS interface adaptors can be configured to operate as passive channel activity monitors (TAP). One or more NTDS Parallel or Serial interface adaptors, in any mix, can be combined to form a complete multichannel monitoring system (Figures 7.1 and 7.2). The passive interface acts as an invisible channel activity observer and does not participate or interact with the connected NTDS port in any way. A comprehensive channel transaction analyzer is created when coupled with available software drivers and application programs (Figure 7.4). The ability to record and display real-time channel activity enables the user to easily isolate and troubleshoot complex communications failures.

7.1.1 GENERAL OPERATIONAL DESCRIPTION

The interface monitors the activity of the NTDS control signals and, when a valid transaction is detected, the corresponding data word, transaction type, and time tag are recorded (Figures 7.5 and 7.6). The TAP monitor begins transaction recording and event data collection based on specific triggering conditions. When this trigger condition is detected the user specified NTDS transactions and other events are collected in real-time and stored in a Data Collection FIFO for transfer to system memory. The recording process continues until it is suspended by the detection of a user specified check or termination condition. The recorded data can be processed in real-time or off line.

7.1.2 NTDS PARALLEL CHANNELS

The GET Parallel Channel NTDS Interface Adaptors have one Receive Port which can always operate as a passive TAP. The standard Transmit Port can not be used for TAP operations. However, most adaptors feature a TAP mezzanine module which allows the Transmit port to operate as a passive TAP. The 32 bit TAP ports can be software configured to operate in NTDS SLOW, FAST, ANEW, or Type H environments and can monitor transactions on Category I, II, or III connections. The typical NTDS TAP block diagram is illustrated in Figure 7.3.

7.1.3 NTDS SERIAL CHANNELS

Two types of NTDS Serial Channel Interface Adaptors allow TAP operation in Type D and Type E environments. These adaptors have two ports which can operate as passive TAPs. These 32 bit NTDS ports can be software configured to operate with all Parity, Control Frame, and SIF options.

7.2 GENERAL OPERATING DESCRIPTION

The TAP operation is identical regardless of system bus (PCI, PMC, PC/104+, cPCI, or VME) or adaptor type (Parallel or Serial). The recording process is divided into five functional steps and closely resembles the operation of a typical logic analyzer (Figure 7.5). These steps include pretrigger transaction recording, trigger word detection and recording, specified transaction recording, check word detection and recording, and post-check transaction recording.
7.2.1 GENERAL TAP OPERATION

The TAP is initially configured to match the interface to which it is connected. These configuration options are software selectable (Table 7.1). Recording trigger, filter, check, and termination parameters are then loaded into the TAP command fields and the TAP is started. Transaction recording starts when the prescribed trigger condition is encountered. A time tag synchronization signal is generated notifying other TAP channels that a trigger condition has been detected. Each transaction is analyzed according to the filtering criteria, and if it is qualified, it is recorded. This recording process continues until a specified check condition is detected. At that time the TAP can be stopped or automatically restarted, based on a set of predefined parameters. A termination signal is generated notifying other TAP channels that a termination condition has been detected. A typical TAP recording session is depicted in Figure 7.6.

7.2.2 TAP DATA FORMATS

Specified NTDS transactions or events are collected, formatted, and loaded into a Data Collection FIFO for transfer to system memory. The TAP recording buffer will contain a detected trigger or sync word, any number of recorded transaction and TAP event words, a possible check word, a possible number of post-check transaction words, and a termination event word. All NTDS transactions are recorded as 32 bit elements. The recorded transaction and event word formatting consists of a 32 bit data field with an appended 24 bit timestamp (100 ns or 125 ns resolution) and an 8 bit status byte. The adaptor dependent status byte describes the transaction recording conditions.

7.3 TAP SOFTWARE DESCRIPTION

The GET NTDS Channel Analyzer System software program, GET 55701741, is available for controlling TAP configured interface adaptors. This full featured Windows (WDM, NT) application program provides all of the functions and utilities which allow the user to fully configure and control the TAP interface. Single and multiple interface adaptor systems are supported. When used with the available Windows NT PCI TAP Driver (GET 50701741), the low order control, configuration, synchronization, and data display functions are handled by the program. Figure 7.4 shows some typical TAP Software screens.

7.4 NTDS PARALLEL CHANNEL OPERATION

An NTDS Parallel channel consists of an Input and an Output Port, each of which contain up to 32 data lines and four control lines. The transfer of data over the NTDS ports is controlled by the operation of these control lines. The operation of these NTDS channels is described in other sections of this document. For a complete description of NTDS data exchange protocols refer to MIL-STD-1397C (SHIPS) Military Standard Document.

7.4.1 PARALLEL CHANNEL TAP OPERATION

The TAP Port records transactions and events based on the activity of the four NTDS control lines. When connected to an NTDS Output Port the transaction information is collected on the low to high transition of the ODA or EFA lines. The EFR line is used to indicate if the transaction was performed with force. When connected to an NTDS Input Port the transaction information is collected on the low to high transition of the IDA line. The IDR, EIR, and EIE lines are used to indicate the type of transfer performed (Figure 7.7).
FIGURE 7.1
NTDS PARALLEL INTERFACE ADAPTOR - TAP CONNECTIONS

FIGURE 7.2
NTDS SERIAL INTERFACE ADAPTOR - TAP CONNECTIONS
GET ENGINEERING CORPORATION

FIGURE 7.6

NTDS TAP RECORDING SESSION

TRANSACTION

EF

OD

EVENT

TRIGGER

RECORD

CHECK

OTHER EVENTS

NOTE 6

ACTION

TAP START

RECORDED TO TAP BUFFER

TRANSACTIONS NOT RECORDED

TAP TRANSACTION RECORDING

TAP RECORD FRAME

POST CHECK RECORDING

TRANSACTIONS NOT RECORDED

NOTES:

1. * DENOTES TRANSACTION WHICH IS QUALIFIED
   BY TYPE, MASK, AND COMPARE REGISTERS
2. TRIGGER WORD DEFINED AS FUNCTION
3. RECORD WORDS DEFINED AS DATA
4. CHECK WORD DEFINED AS FUNCTION
5. POSTCHECK RECORDING LENGTH = 4
6. OTHER EVENTS MAY BE:
   INTERWORD TIMEOUT, SYNC, SIF ERROR,
   TIMESTAMP OVERFLOW, TAP STOP, ETC.

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9350 BOND AVENUE
EL CAJON, CA 92019

NTDS TAP DATA

GET 10010501

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7.5 NTDS SERIAL CHANNEL OPERATION

An NTDS Serial channel consists a Sink and a Source Port, each of which transacts 32 bit information and 3 or 4 bit control frames. The transfer of serial information frames is controlled by the operation the control frames. The operation of these NTDS channels is described in detail in other sections of this document. For a complete description of NTDS serial data exchange protocols refer to MIL-STD-1397C (SHIPS) Military Standard Document.

7.5.1 SERIAL CHANNEL TAP OPERATION

The Sink and Source Ports can be used to passively record transactions between two other NTDS devices. The serial TAP it records transactions based on the presence of SWT or Burst IFs. The SIS and SOS control frames are used only in the evaluation of SIF errors. Control frame formats, IF parity, and timing parameters can be specified by the user. Transaction information is collected after the entire IF is received (Figure 7.8).

7.6 TAP EVENT DETECTION

The TAP operation is controlled by a set of registers which define the operating parameters for performing transaction and event detection and recording. Among these registers are the interword and buffer timers, and the Trigger, Record, and Check mask registers.

7.6.1 TRIGGER COMPARE AND MASK

The Trigger Compare and Mask Registers specify the data field portion of the TAP trigger event. All detected transactions are tested to see if they satisfy the defined trigger condition. This evaluation criteria includes transfer type and data field pattern matching. A trigger condition exists and transaction recording can begin if a type and data field match are found. The set bits in the Trigger Mask Register specify which bits in the Trigger Compare Register will be used when performing the data field pattern match.

7.6.2 RECORD COMPARE AND MASK

The Record Compare and Mask Registers specify the data field TAP recording filter. This filter is used during all Record and Post-termination recording operations. All detected transactions are tested to see if they satisfy the defined recording conditions. This evaluation criteria includes transfer type and data field pattern matching. A recording condition exists if a type and data field match are found. The set bits in the Record Mask Register specify which bits in the Record Compare Register will be used when performing the data field pattern match.

7.6.3 CHECK COMPARE AND MASK

The Check Compare and Mask Registers specify the data field data field portion of the TAP check event. All detected transactions are tested to see if they satisfy the defined check conditions. This evaluation criteria includes transfer type and data field pattern matching. A check condition exists and Post-check transaction recording can begin if a type and data field match are found. The set bits in the Check Mask Register specify which bits in the Check Compare Register will be used when performing the data field pattern match.
7.7 **TAP TIMEOUTS**

The TAP contains several timers which provide event detection based on several timeout conditions. When specified, the timeout events are recorded into the TAP buffer. Additionally, the timeout events can also specify a TAP termination condition. The operation of these timeouts are illustrated in the TAP Functional Flow Diagram, Figure 7.6.

7.7.1 **COMMAND TIMEOUT**

The Command Timer is 32 bit counter based on a 1 microsecond clock and provides a method of terminating the TAP after a specified period has expired. The Command timer can optionally be configured as a Buffer period timer. The Command Timer is initialized with the specified timeout period and started when the TAP is started. When configured as a Buffer timer the counter is started after the first NTDS transaction is detected after the TAP is started. If the Command Timer expires before any other defined terminating condition is detected, the TAP session will be terminated, regardless of operational state.

7.7.2 **INTERWORD TIMEOUT**

The Interword Timer is 16 bit counter based on a selectable 1 microsecond or 1 millisecond clock. An Interword Timeout event can be specified to terminate a current Record or Post-terminate recording operation. The interword timer is initialized and started when a transaction is detected. An interword timeout is declared if this timer expires before the next transaction is detected. When the interword timeout occurs a TAP event is recorded and the TAP frame or recording session can be optionally stopped.

7.7.3 **SIF ERRORS**

The Serial Interface adaptors can be configured to generate a TAP recording event when a SIF error (IF format, control frame format, or protocol sequence) is detected. The actual control frames are not recorded and the SIF error event is reported in the Status Byte and timestamp fields of the recording word. A protocol sequence error is declared if consecutive control frames with the same ID bits are detected. Additionally, a SIF recording event will be declared if an IF error (framing, sync, or parity) or control frame error (framing or sync) is detected. The TAP frame or recording session can be terminated when a SIF error is detected.

7.8 **TAP EVENT RECORDING**

All TAP events are recorded in the order in which they are received. The timestamp is reset after each event is recorded and represents the time elapsed since the previously recorded TAP event. A typical TAP recording session is depicted in Figure 7.6. The typical TAP recording session buffer may contain one or more TAP Recording Frames, depending upon selected retrigger and termination options. Each TAP Recording Frame consists of a number of a detected trigger transaction and/or an external synch event, a number of recorded transactions and TAP events, a possible check transaction or event, a possible number of post-check transactions and events, and a TAP stop/restart event word.
### TABLE 7.1

#### CONFIGURATION OPTIONS

<table>
<thead>
<tr>
<th>NTDS CATEGORY</th>
<th>OPTION</th>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT</td>
<td>TAP CPU INPUT FROM PERIPHERAL INTERFACE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUTPUT</td>
<td>TAP CPU OUTPUT TO PERIPHERAL INTERFACE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NTDS TYPE</td>
<td>SLOW</td>
<td>NTDS SLOW ( -15 VOLT NOM ) OPERATION</td>
<td></td>
</tr>
<tr>
<td></td>
<td>FAST</td>
<td>NTDS FAST ( -3 VOLT NOM ) OPERATION</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ANEW/H</td>
<td>NTDS ANEW OR TYPE H ( +3 VOLT NOM ) OPERATION</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>OPTION</th>
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<th>DESCRIPTION</th>
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<tr>
<td>PARITY</td>
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</tr>
<tr>
<td>ODD</td>
<td>SERIAL DATA PARITY IS ODD</td>
<td></td>
</tr>
<tr>
<td>EVEN</td>
<td>SERIAL DATA PARITY IS EVEN</td>
<td></td>
</tr>
<tr>
<td>NONE</td>
<td>SERIAL DATA HAS NO PARITY BIT</td>
<td></td>
</tr>
<tr>
<td>CONTROL FRAME</td>
<td>0 OR 1</td>
<td></td>
</tr>
<tr>
<td>SIS ID</td>
<td>0 OR 1</td>
<td></td>
</tr>
<tr>
<td>SOS ID</td>
<td>0 OR 1</td>
<td></td>
</tr>
<tr>
<td>SIF</td>
<td>SIFEN</td>
<td>1 = SIF TESTING ENABLED. 0 = DISABLED</td>
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<th>OPTION</th>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ERROR TESTING AVAILABLE FOR TYPE D ADAPTORS</td>
<td></td>
</tr>
</tbody>
</table>

**TABLE 7.1**

**CONFIGURATION OPTIONS**

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<thead>
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</tr>
<tr>
<td>NONE</td>
<td>SERIAL DATA HAS NO PARITY BIT</td>
<td></td>
</tr>
<tr>
<td>CONTROL FRAME</td>
<td>0 OR 1</td>
<td></td>
</tr>
<tr>
<td>SIS ID</td>
<td>0 OR 1</td>
<td></td>
</tr>
<tr>
<td>SOS ID</td>
<td>0 OR 1</td>
<td></td>
</tr>
<tr>
<td>SIF</td>
<td>SIFEN</td>
<td>1 = SIF TESTING ENABLED. 0 = DISABLED</td>
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<td></td>
<td>ERROR TESTING AVAILABLE FOR TYPE D ADAPTORS</td>
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</table>
FIGURE 7.7
PARALLEL CHANNEL TAP TIMING

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PROPOSED TAP TIMING

NTDS COMPUTER INPUT PORT

IDR

INPUT DATA [000-311]

IDR

IDM

EIR

EIE

NTDS PERIPHERAL INPUT PORT

TAP CABLE T-BOX

INPUT DATA [000-311]

OoR

ODA

EIR

EIE

IDM

EIE

TRANSACTION SAMPLED

TRANSACTION SAMPLED

NTDS TAP INPUT PORT

TAP CONNECTOR TRANSITION MODULE

IDR

ODA

EIR

EFR

OUTPUT DATA [000-311]

ODA

ODR

EFR

EIR

EFR

NTDS COMPUTER OUTPUT PORT

NTDS PERIPHERAL OUTPUT PORT

COMPUTER INPUT PORT TAP CONNECTION AND TIMING

COMPUTER OUTPUT PORT TAP CONNECTION AND TIMING

INPUT DATA [000-311]

DATA VALID

DATA VALID

OUTPUT DATA [000-311]

OUTPUT DATA [000-311]
FIGURE 7.8
SERIAL CHANNEL TAP TIMING

NTDS SERIAL TAP

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NTDS SERIAL TAP TIMING
SECTION 8
NTDS INTERFACE
CONNECTORS AND CABLES

8.1 NTDS CABLES

The maximum cable length allowed depends on the cable and the interface type (Table 8.1). The maximum lengths indicated are those for which proper operation is assured for equipment otherwise fully conforming to the NTDS specification. The interface circuits used in GET NTDS interface adaptors are designed to support much longer cable lengths. However, each system interface must be individually analyzed for proper operation with longer cables. Issues regarding buffer timeouts, transaction interword timeouts, and other possible problems caused by the additional delays caused by longer cables must be addressed. The following description of NTDS cables and connectors is intended only as an aid in explaining possible interconnection schemes and does not cover all aspects of NTDS connectivity. For a complete description of NTDS cables and connectors refer to MIL-STD-1397C (NAVY) Military Standard Document.

8.1.1 INDUSTRY STANDARD CABLES

Due to the high cost and relatively long lead times for LS2U-45 shipboard cable many shore based or development NTDS installations are opting for the use of commercial cable equivalents. However, under most conditions commercial cable is not recommended for shipboard installations. GET produces a commercial grade cable that has equivalent electrical characteristics as the 2U cable. This 37 conductor pair, PVC jacketed cable has the advantage of being highly flexible while maintaining a 100% metal braid shield, and a mylar foil shield with open drain wire and is completely suitable for most NTDS applications. Complete specifications for the GET 46523437 cable are shown in Figure 8.1.

8.2 NTDS CONNECTORS

The connectors used on NTDS parallel interface systems are keyed to prevent improper connection. By convention the references to input and output are with respect to the computer. The computer input cabinet connector may be the same as the peripheral equipment output cabinet connector. The computer output cabinet connector may be the same as the peripheral equipment input cabinet connector. This configuration, if the same family of connectors is used, allows the Input cables to be interchanged with the Output cables by turning them end for end. The recommended cabinet and cable connectors are listed in Table 8.2.

8.2.1 INDUSTRY STANDARD PARALLEL CONNECTORS

Commercial ribbon cable systems are typically used for most development and shore based systems. Ribbon cables are not recommended for shipboard installations. GET produces a complete line of transition modules that allow quick ribbon cable connections to NTDS devices. These compact modules feature high density 80 contact ribbon cable connectors which are compatible with all GET NTDS products. These easily interchangeable cable transition modules enable efficient system reconfiguration and troubleshooting.
8.2.2 INDUSTRY STANDARD SERIAL CONNECTORS

The physical requirements placed on most commercial interface adaptors require the use of relatively small connectors. The large NTDS serial interface coax and triax connectors are typically too large to fit in most commercially packaged computer systems. This has led the industry to shift to smaller electrically equivalent connectors, as listed in Table 8.2.

8.3 NTDS CONNECTOR SIGNAL ASSIGNMENTS

The standard function to connector pin assignments for the connectors listed in Table 8.2 are listed in Table 8.3. Pins not listed may have no connections. The standard cable wire pair color code must be used to facilitate connector maintenance and guarantee signal integrity.

8.4 ATDS CONNECTOR SIGNAL ASSIGNMENTS

A front panel mounted 25 contact connectors are used as the ATDS serial interface for standard GET ATDS products. The connectors used and their recommended mating cable connector are listed below. Unless otherwise specified, the GET ATDS interface features bidirectional transceivers. These transceivers are configured as drivers or receivers, depending on the operating mode (DTS or TDS CPU). Unused signals should be left open (not connected). The signal pin assignments and the transceiver modes for the ATDS interface connector are listed in Table 8.4.

<table>
<thead>
<tr>
<th>QUALITY</th>
<th>MANUFACTURER</th>
<th>FRONT PANEL SOCKET CONNECTOR</th>
<th>MATING CABLE PLUG CONNECTOR W/18&quot; WIRED LEADS</th>
<th>MATING CABLE PLUG CONNECTOR SOLDER / CRIMP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>CANNON</td>
<td>DB25-S</td>
<td>-</td>
<td>DB25-P</td>
</tr>
<tr>
<td>Commercial</td>
<td>CANNON</td>
<td>MDSM-25SC-210-VR17</td>
<td>CA111972-12</td>
<td>MDSM-25SC-211-VS1</td>
</tr>
<tr>
<td>Commercial</td>
<td>MOLEX</td>
<td>83614-9012</td>
<td>83424-9019</td>
<td>83424-9014</td>
</tr>
<tr>
<td>Military</td>
<td>CANNON</td>
<td>MDM-25SBRP-T</td>
<td>M83513/03D01C</td>
<td>M83513/01DC</td>
</tr>
</tbody>
</table>
### Table 8.1
MAXIMUM NTDS CABLE LENGTHS

<table>
<thead>
<tr>
<th>INTERFACE TYPE</th>
<th>NTDS CABLE TYPE</th>
<th>PARALLEL INTERFACE SYSTEMS</th>
<th>SERIAL INTERFACE SYSTEMS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>2U OR 2UW OR LS2U</td>
<td>RG/12A</td>
</tr>
<tr>
<td>A</td>
<td>300 FT 91.4 METERS</td>
<td>300 FT 91.4 METERS</td>
<td>D 1000 FT 304.8 METERS</td>
</tr>
<tr>
<td>B</td>
<td>50 FT 15.2 METERS</td>
<td>150 FT 45.7 METERS</td>
<td>MIL-C-17/135 TRF-8</td>
</tr>
<tr>
<td>C</td>
<td>100 FT 30.5 METERS</td>
<td>250 FT 76.2 METERS</td>
<td>MIL-C-17/134 TRF-58</td>
</tr>
<tr>
<td>H</td>
<td>100 FT 30.5 METERS</td>
<td>250 FT 76.2 METERS</td>
<td>E 985 FT 300 METERS</td>
</tr>
</tbody>
</table>

### Table 8.2
NTDS CONNECTORS

<table>
<thead>
<tr>
<th>NTDS TYPE</th>
<th>COMMON NAME</th>
<th>NUMBER OF CONTACTS</th>
<th>PORT</th>
<th>CABINET CONNECTOR</th>
<th>CABLE CONNECTOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>A, B, C, H</td>
<td>UYK/20</td>
<td>120</td>
<td>INPUT</td>
<td>GET 45121120</td>
<td>7101943-02</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>OUTPUT</td>
<td>GET 45121121</td>
<td>7101943-01</td>
</tr>
<tr>
<td>A, B, C, H</td>
<td>UYK/43</td>
<td>92</td>
<td>INPUT</td>
<td>M28840/12AG1P1</td>
<td>M28840/16AG1S1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>OUTPUT</td>
<td>M28840/12AG1P2</td>
<td>M28840/16AG1S2</td>
</tr>
<tr>
<td>A, B, C, H</td>
<td>DPD90 CP-642</td>
<td>90</td>
<td>INPUT</td>
<td>DPD-90-34P</td>
<td>DPD-90-33S</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>OUTPUT</td>
<td>DPD-90-34P</td>
<td>DPD-90-33S</td>
</tr>
<tr>
<td>A, B, C, H</td>
<td>UYK/7</td>
<td>85</td>
<td>INPUT</td>
<td>M81511/01EF01P1</td>
<td>M81511/06EF01S1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>OUTPUT</td>
<td>M81511/01EF01P2</td>
<td>M81511/06EF01S2</td>
</tr>
<tr>
<td>A, B, C, H</td>
<td>UYK/44</td>
<td>79</td>
<td>INPUT</td>
<td>D38999/20WG35P</td>
<td>D38999/26WG35SN</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>OUTPUT</td>
<td>D38999/20WG35P</td>
<td>D38999/26WG35SA</td>
</tr>
<tr>
<td>D</td>
<td>SERIAL</td>
<td>COAX</td>
<td>MIL</td>
<td>COMMERCIAL UCBBJR-26</td>
<td>PL20-7</td>
</tr>
<tr>
<td>E</td>
<td>LOW LEVEL SERIAL</td>
<td>TRIAX</td>
<td>MIL</td>
<td>M49141/1-0001</td>
<td>M49141/1-0002</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIL</td>
<td>M49142/2-0001</td>
<td>M49141/1-0002</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>COMMERCIAL BJ-77</td>
<td>PL75C-7</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>COMMERCIAL BJ-80</td>
<td>PL80-7</td>
<td></td>
</tr>
</tbody>
</table>
FIGURE 8.1 GET CABLE SPECIFICATION

NOTES
- 37 TWISTED PAIRS (24 AWG T/32 TINNED COPPER)
- .049" SR-PVC INSULATION
- OVERALL ALUMINUM MYLAR SHIELD
- 36 AWG TINNED COPPER BRAID (95% MIN. COVERAGE)
- .005" PVC OUTER JACKET
- NOMINAL O.D. .060" +/- .005"
- CHARACTERISTIC IMPEDANCE FOR EACH WIRE PAIR = 51.28 OHMS PER 1000 FEET
- UL 2243 APPROVED
- 3.0" BEND RADIUS (30 D.I.G., BEND)
- SUITABLE FOR MOST TEMPEST APPLICATIONS
## Table 8.3

### MIL-STD-1397 (NAVY) Cable Pin Assignments

<table>
<thead>
<tr>
<th>Connector</th>
<th>3-M Hole</th>
<th>Molex</th>
<th>AMPHENOL</th>
<th>DUNPT</th>
<th>MIL-STD-1397C Specified Connectors</th>
</tr>
</thead>
<tbody>
<tr>
<td>CABLE OUTPUT</td>
<td>3452-6560</td>
<td>52759-1200</td>
<td>848-CR</td>
<td>8064x</td>
<td>50637-1124</td>
</tr>
<tr>
<td>CABLE INPUT</td>
<td>3414-6634</td>
<td>52759-1000</td>
<td>848-50x</td>
<td>8064x</td>
<td>50637-1124</td>
</tr>
<tr>
<td>PANEL OUTPUT</td>
<td>3433-6320</td>
<td>52759-1200</td>
<td>848-50x</td>
<td>8064x</td>
<td>50637-1124</td>
</tr>
<tr>
<td>PANEL INPUT</td>
<td>3431-6320</td>
<td>52759-1000</td>
<td>848-50x</td>
<td>8064x</td>
<td>50637-1124</td>
</tr>
</tbody>
</table>

### NTDS Cables & Color Codes

<table>
<thead>
<tr>
<th>Type of Length</th>
<th>MIL-STD-1397C Specified Connectors</th>
</tr>
</thead>
<tbody>
<tr>
<td>A 300</td>
<td>MIL-C-24643</td>
</tr>
<tr>
<td>B 50</td>
<td>MIL-C-24643</td>
</tr>
<tr>
<td>C/H 100</td>
<td>MIL-C-24643</td>
</tr>
</tbody>
</table>

### Get NSN's of the MIL-STD-1397C NTDS INTERFACE - Get 10010504

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## TABLE 8.4
ATDS CONNECTOR PIN ASSIGNMENTS

<table>
<thead>
<tr>
<th>SIGNAL NAME</th>
<th>SIGNAL</th>
<th>RETURN</th>
<th>DTS MODE</th>
<th>TDS MODE</th>
<th>CIRCUIT TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHIELD</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>Transformer</td>
</tr>
<tr>
<td>FRAME</td>
<td>14</td>
<td>2</td>
<td>Driver</td>
<td>Receiver</td>
<td>Transformer</td>
</tr>
<tr>
<td>INCOMING DATA</td>
<td>15</td>
<td>3</td>
<td>Driver</td>
<td>Receiver</td>
<td>Transformer</td>
</tr>
<tr>
<td>OUTGOING DATA</td>
<td>16</td>
<td>4</td>
<td>Receiver</td>
<td>Driver</td>
<td>Transformer</td>
</tr>
<tr>
<td>DATA CLOCK</td>
<td>17</td>
<td>5</td>
<td>Receiver</td>
<td>Driver</td>
<td>Transformer</td>
</tr>
<tr>
<td>ADDRESS DATA</td>
<td>18</td>
<td>6</td>
<td>Receiver</td>
<td>Driver</td>
<td>Transformer</td>
</tr>
<tr>
<td>ADDRESS CLOCK</td>
<td>19</td>
<td>7</td>
<td>Receiver</td>
<td>Driver</td>
<td>Transformer</td>
</tr>
<tr>
<td>NET CONTROL</td>
<td>8</td>
<td>20</td>
<td>Driver</td>
<td>Receiver</td>
<td>10 Volt</td>
</tr>
<tr>
<td>SIDETONE FRAME</td>
<td>9</td>
<td>21</td>
<td>Driver</td>
<td>Receiver</td>
<td>TTL</td>
</tr>
<tr>
<td>SIDETONE DATA</td>
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<td>22</td>
<td>Driver</td>
<td>Receiver</td>
<td>TTL</td>
</tr>
<tr>
<td>SIDETONE CLOCK</td>
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<td>23</td>
<td>Receiver</td>
<td>Driver</td>
<td>TTL</td>
</tr>
<tr>
<td>NO CONNECTION</td>
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<td>24</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NO CONNECTION</td>
<td>13</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:** CIRCUIT TYPES

- TRANSFORMER = 6 Volt P/P, 100 Ohm Load - TRANSFORMER COUPLED
- 10 VOLT = 10 Volt DC INTERFACE - DIRECT CONNECTION
- TTL = TTL LOGIC LEVEL - DIRECT CONNECTION