



GENERAL DISCUSSION
of the
NTDS PARALLEL INTERFACE

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GET NTDS PARALLEL INTERFACE DESCRIPTION

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SECTION 1
NTDS PARALLEL INTERFACE
DISCUSSION

1.1 SCOPE

This document contains information discussing the general design philosophy used in implementation of GET NTDS PARALLEL Interface Adaptors. This document is intended to assist qualified personnel in the development, operation, installation, and diagnosis of these adaptors. It is not the intent or purpose of this document to define the actual uses or applications of NTDS interfaces. Programming and application examples or outlines and diagrams which may be found in this document are intended only to illustrate the operation of the NTDS interface.

1.2 NTDS OVERVIEW

The GET NTDS Interface Adaptors can be configured to operate as NTDS Peripheral or Computer channel devices. Each CHANNEL consists of an Input and an Output Port, each of which contain up to 32 data lines and four control lines. The transfer of information is controlled by these control lines. The following description of the operation of an NTDS channel is intended only as an aid in explaining the interface operation of the typical NTDS interface and as such does not cover all aspects of NTDS protocols. For a complete description of NTDS information exchange protocols refer to MIL-STD-1397C (SHIPS) Military Standard Document.

1.2.1 NTDS INTERFACES

There are four Types of NTDS Parallel interfaces specified, each of which can operate in three Categories. The NTDS TYPE defines the electrical interface characteristics while the CATEGORY describes the signal timing protocol used for information exchange operations.

1.2.2 PARALLEL INTERFACE CATEGORIES

The GET NTDS parallel interface ports are individually configurable to operate as Computer or Peripheral channels. This enables a single interface adaptor to operate in any one of the three NTDS equipment categories defined in MIL-STD-1397C. These equipment categories are:

- A. Category I - Computer to Peripheral
- B. Category II - Computer to Computer (Inter-Computer)
- C. Category III - Peripheral to Peripheral (Inter-Peripheral)

In Category 2 mode the Output port operates as a Peripheral and the Input port operates as a Computer. In Category 3 mode the Output port operates as a Computer and the Input port operates as a Peripheral. In the Passive Monitor mode the Output port is disabled and the Input port records the transfers between two other NTDS devices. Additionally, the Computer mode interfaces can be configured to operate in interlocked or pulsed modes.

1.2.3 PARALLEL INTERFACE TIMING

The actual state (logic 1 or 0) of the NTDS Data lines is determined by their DC voltage level, and do not have to be cleared between successive transactions. The only restriction is that the Data lines must be stable during the time that the associated control lines indicate data validity. The control signals are edge significant and the receiving device must be able to recognize their change of state (from logic 1 to 0 or 0 to 1) accordingly. The receiving device must not recognize a subsequent logical 1 until that line has first transitioned to a logic 0 state.

1.2.4 PARALLEL INTERFACE TYPES

The parallel interface adaptor channels can be configured to operate in NTDS TYPE A (SLOW), TYPE B (FAST), TYPE C (ANEW), or TYPE H (HIGH THROUGHPUT) mode. A special TRISTATE (OPEN CABLE) mode is also possible.

1.2.4.1 TYPE A (SLOW)

In Type A mode, also called SLOW, transfer rates of 41.67 K words per second on one cable are possible. Nominal voltage levels of 0.0 VDC (logic 1), -15 VDC (logic 0), and switching thresholds of -6 VDC are used. Controlled slew rate driver outputs with linear characteristics are required. The receiver circuits must be able to reject single ended input transient pulse signals with specific maximum energy levels. The receiver outputs must be logic 0 for all open input conditions. Maximum specified cable lengths are 300 ft.

1.2.4.2 TYPE B (FAST)

In Type B mode, also called FAST, transfer rates of 250 K words per second on one cable are possible. Nominal voltage levels of 0.0 VDC (logic 1), -3 VDC (logic 0), and switching thresholds of -1.5 VDC are used. The referenced input receiver circuits must be able to reject common mode input transient pulse or DC signals. The receiver outputs must be logic 0 for all open input conditions. Controlled slew rate driver outputs are required. Depending on type of cable, used maximum specified cable lengths are 50 or 100 ft.

1.2.4.3 TYPE C (ANEW)

In Type C mode, also called ANEW, transfer rates of 250 K words per second on one cable are possible. Nominal voltage levels of 0.0 VDC (logic 1), +3.5 VDC (logic 0), and switching thresholds of +1.5 VDC are used. The referenced input receiver circuits must be able to reject common mode input transient pulse or DC signals. The receiver outputs must be logic 0 for all open input conditions. Controlled slew rate driver outputs are required. Depending on type of cable used, maximum specified cable lengths are 100 or 250 ft.

1.2.4.4 TYPE H (HIGH THROUGHPUT)

In Type H mode, also called HIGH THROUGHPUT or FAST ANEW, transfer rates of 500 K words per second on one cable are possible. Nominal voltage levels of 0.0 VDC (logic 1), +3.5 VDC (logic 0), and switch thresholds of +1.5 VDC are used. The referenced input receiver circuits must be able to reject common mode input transient pulse or DC signals. The receiver outputs must be logic 0 for all open input conditions. Controlled slew rate driver outputs are required. Depending on type of cable used, maximum specified cable lengths are 100 or 250 ft.

1.2.4.5 TRISTATE (OPEN CABLE)

The GET NTDS parallel interface adaptor channels can also be configured to operate in the TRISTATE mode. In this mode the driver circuits are placed in a high impedance state approximating an open cable. Among other capabilities, this feature makes it possible to install a 'hot spare' adaptor in parallel with an active adaptor.

1.3 CATEGORY I OUTPUT PORT OPERATION

Transfer of information between NTDS computers and peripherals is accomplished in two major methods: Data and Functions. The Output Port transactions are controlled by the Peripheral's request (ODR and EFR) lines and the Computer's acknowledge (ODA and EFA) lines. Either one or both of the peripheral's request lines may be activated. However, only one of the computer's acknowledge lines may be active at any one time.

1.3.1 OUTPUT DATA TIMING

A peripheral device sets its Output Request (ODR) line when it is in a condition to accept an Output Data (OD) word from the NTDS computer. The computer responds, at its convenience, by activating its Output Acknowledge (ODA) line. The active ODA line indicates to the peripheral device that the data contained on the OD lines is valid and should be sampled. The peripheral device acknowledges the receipt of data by deactivating its ODR line. Figure 1.1 illustrates the control signal timing relationships for Output Data transfers.

1.3.2 EXTERNAL FUNCTION TIMING

A peripheral device sets its External Function Request (EFR) line when it is in a condition to accept an External Function (EF) command word from the NTDS computer. The computer responds, at its convenience, by activating its External Function Acknowledge (EFA) line. The active EFA line indicates to the peripheral device that the command word contained on the OD lines is valid and should be sampled. The peripheral device acknowledges the receipt of data by deactivating its EFR line. Figure 1.2 illustrates the control signal timing relationships for External Function transactions.

1.3.2.1 FORCED EXTERNAL FUNCTION TIMING

Some NTDS computers have the ability of sending External Functions with Force. These transfers require no request (EFR) from the peripheral device. The computer, at its convenience, activates its External Function Acknowledge (EFA) line, indicating to the peripheral device that the command word contained on the OD lines is valid and should be sampled. The EFR line is not monitored during the Forced EF. The peripheral device has no control over the rate at which Forced EFs are sent.

1.4 CATEGORY I INPUT PORT OPERATION

Transfer of information between NTDS computers and NTDS peripherals is accomplished in two major methods: Data and Interrupts. The Input Port transactions are controlled by the Peripheral Device's request (IDR and EIR) lines and the Computer's Input Acknowledge (IDA) and Interrupt Enable (EIE) lines. Only one of the peripheral's request lines may be activated at any one time.

1.4.1 INPUT DATA TIMING

An active Input Data Request (IDR) line indicates to the computer that the peripheral has placed valid data on the Input port data lines. The NTDS Computer Input Data Acknowledge (IDA) line indicates to the peripheral device that the computer has sampled this data. When the peripheral device senses that the IDA line is active it deactivates its IDR line. When the computer deactivates its IDA line the input cycle is complete. Figure 1.3 illustrates Input Port control signal timing.

1.4.2 EXTERNAL INTERRUPT TIMING

Transmission of External Interrupt words from the peripheral device to the computer is controlled by the External Interrupt Enable (EIE) line. When sending an External Interrupt the peripheral device activates its External Interrupt Request (EIR) line indicating the validity of the interrupt data on the Input data lines. At its convenience the NTDS computer accepts the interrupt code, deactivates its EIE line and activates its IDA line. The peripheral device senses that the IDA line is active and responds by deactivating its EIR line. When the computer deactivates its IDA line the input cycle is complete. That not all computers have an EIE line and peripheral equipment may be designed to initiate an External Interrupt transfer without monitoring the EIE line. This does not, however, alter the timing sequence since the computer will still accept the interrupt at its own convenience using the IDA line. Refer to Figure 1.4.

1.5 NTDS CHANNEL IMPLEMENTATION

The MIL-STD-1397C (Ships) Specification allows a wide variation in the implementation of NTDS channel interface designs. This allows the designer to develop circuits which will maximize the total system channel throughput. The GET NTDS channels are designed to take full advantage of these modes. The three main design schemes currently used are:

- A. Interlocked
- B. Pipeline
- C. Pulse

1.5.1 INTERLOCKED OPERATION

The interlocked mode timing allows the channel to operate at full transfer rates by allowing the peripheral device to satisfy its request line minimum low time during the computer acknowledge line minimum pulse width and data hold times. This feature also has the advantage of allowing the cable control line propagation delays to occur during the acknowledge pulse width and hold times, where they can not affect total system throughput.

1.5.1.1 INTERLOCKED OUTPUT TIMING

A peripheral device sets its Request (ODR or EFR) lines when it is in a condition to accept an Output from the computer. The computer responds, at its convenience, by activating its Output Acknowledge line, indicating that the data is valid. The peripheral samples the data and deactivates its Request line. The computer continues to maintain its acknowledge line active until the minimum pulse width time has expired or, if the peripheral device has not yet deactivated the Request line, until the request line is deactivated (whichever comes last). The Output cycle is complete when the computer deactivates its acknowledge line. Figures 1.1 and 1.2 illustrate control signal timing relationships for Output transactions.

1.5.1.2 INTERLOCKED INPUT TIMING

When the peripheral device wishes to send information to the computer it activates an Input Request (IDR or EIR). The computer samples the data lines and activates the Input Data Acknowledge (IDA). When the peripheral device senses that the IDA line is active it deactivates its IDR line. The computer continues to maintain its IDA line active until the minimum pulse width time has expired or, if the peripheral device has not yet deactivated the Input Request line, until the request line is deactivated (whichever comes last). When the computer deactivates its IDA line the input cycle is complete. Figures 1.3 and 1.4 illustrate the Input control signal timing.

1.5.2 PIPELINE MODE

The pipelined mode timing enables a channel to operate at full transfer rates by allowing the peripheral device to request the next transfer during the closing phase of the current transaction. This is possible because the peripheral's request line minimum low time can then be satisfied during the computer acknowledge minimum pulse width times, and then reactivated, requesting the next transfer even before the original acknowledge pulse width has expired. This feature also allows the cable control line propagation delays to occur during the acknowledge pulse width and hold times, where they may not affect total system throughput. Pipelined timing is illustrated in Figure 1.5.

1.5.2.1 PIPELINED OUTPUT TIMING

A peripheral device sets its Request (ODR or EFR) lines when it is in a condition to accept an Output from the computer. The computer responds by activating its Output Acknowledge line. The peripheral samples the data, deactivates its Request line, and starts a Request line inactive timer. The computer continues to maintain its acknowledge line active until its minimum pulse width time has expired. The peripheral device, after its minimum low time has been satisfied, reactivates the Request line, regardless of the condition of the computer acknowledge line. When the computer deactivates its acknowledge line the current output cycle is complete, and if the request line is active, the new cycle can begin immediately.

1.5.2.2 PIPELINED INPUT TIMING

When the peripheral wishes to send information to the computer it activates an Input Request (IDR or EIR). The computer samples the data lines and activates the Input Data Acknowledge (IDA). When the peripheral device senses that the IDA line is active it deactivates its Request line, and starts a Request line inactive timer. The computer continues to maintain its IDA line active until the minimum pulse width time has expired. The peripheral device, after its minimum low time has been satisfied, presents a new data word and reactivates the Input Request line, regardless of the condition of the computer acknowledge line. When the computer deactivates its IDA line the current input cycle is complete, and if the request line is active, the new cycle can begin immediately.

1.5.3 PULSED MODE

The pulsed operating mode timing is similar to that of the interlocked mode with the exception that the peripheral device is designed to maintain its request lines active as long as the computer acknowledge lines are active. This timing relationship generally does not allow the channel to operate at full transfer rates because the peripheral device can not request the next transfer until the current transfer cycle is complete. Cable delays can not be hidden in the acknowledge portion of the transfer cycles and, therefore, system throughput is affected by cable length. Typical pulsed mode timing is illustrated in Figure 1.6.

1.5.3.1 PULSED OUTPUT TIMING

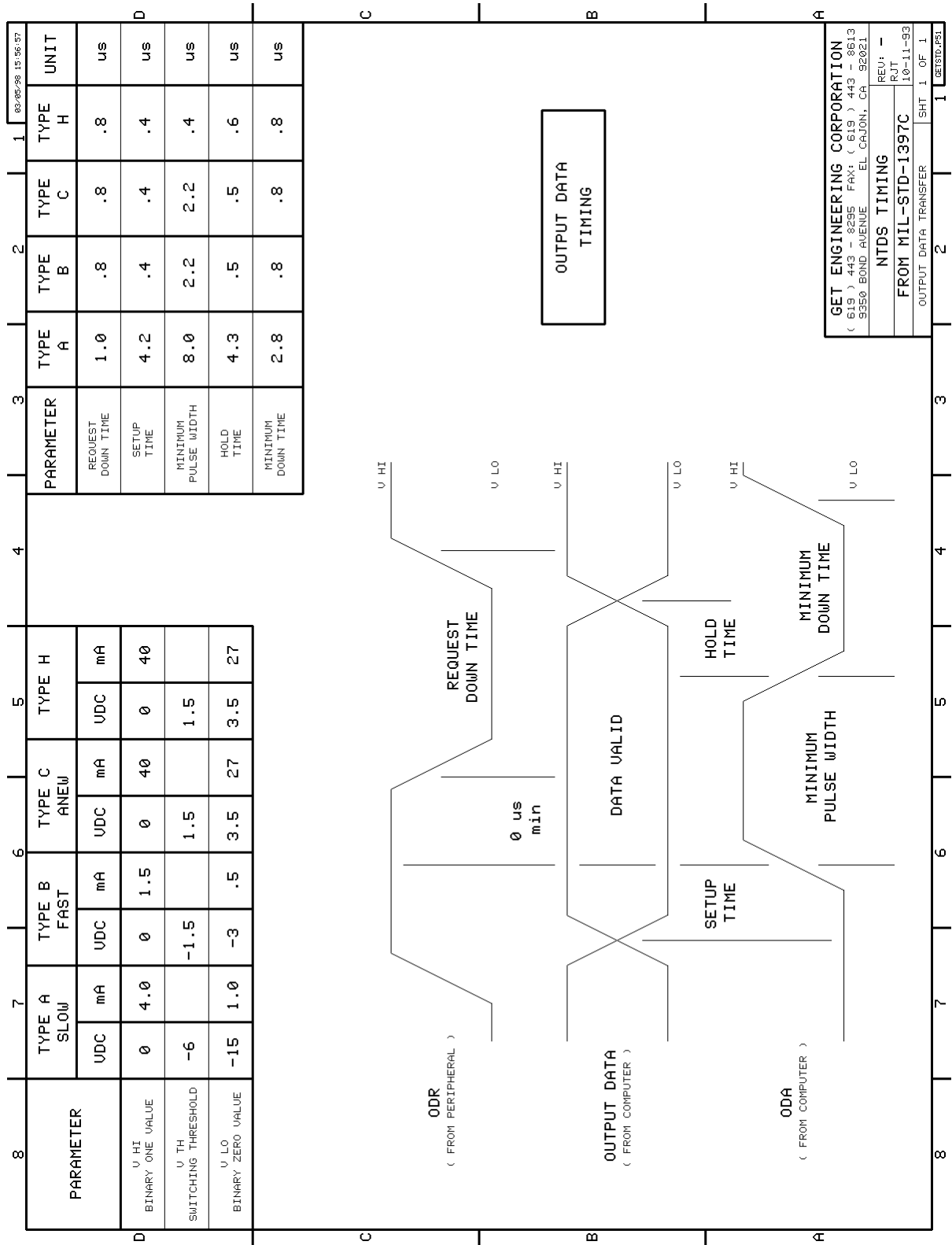
A peripheral device sets its Request (ODR or EFR) lines when it is in a condition to accept an Output from the NTDS computer. The computer responds by activating its Output Acknowledge line and maintaining it active until its minimum pulse width time has expired. The computer then deactivates the acknowledge line. The peripheral device then deactivates its Request line ending current output cycle. The peripheral device can reactivate the Request line and start the next cycle only after its request line minimum low time has been satisfied.

1.5.3.2 PULSED INPUT TIMING

When the peripheral wishes to send information to the computer it activates an Input Request line. The computer samples the data lines and activates the Input Data Acknowledge which remains active until the minimum pulse width time has expired. The computer then deactivates the acknowledge line. When the peripheral senses that the acknowledge line is inactive it deactivates its Request line ending input cycle. The peripheral device can reactivate the Request line and start the next cycle only after its request line minimum low time has been satisfied.

FIGURE 1.1

OUTPUT DATA TIMING



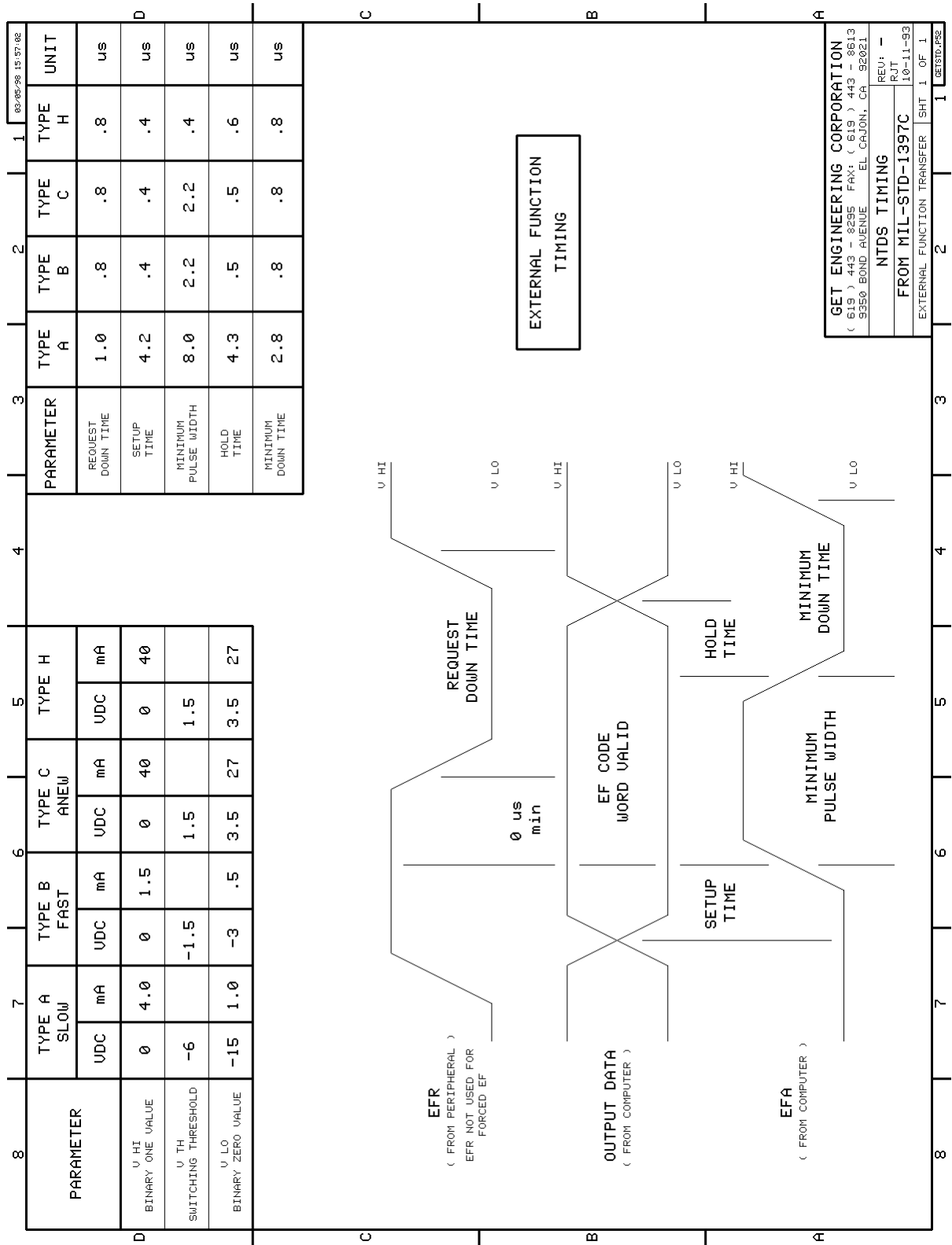
GET ENGINEERING CORPORATION
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 9350 BOND AVENUE EL CAJON, CA 92021

NTDS TIMING
 REV: -
 RUT

FROM MIL-STD-1397C 10-11-93
 OUTPUT DATA TRANSFER SHT 1 OF 1

FIGURE 1.2

EXTERNAL FUNCTION TIMING



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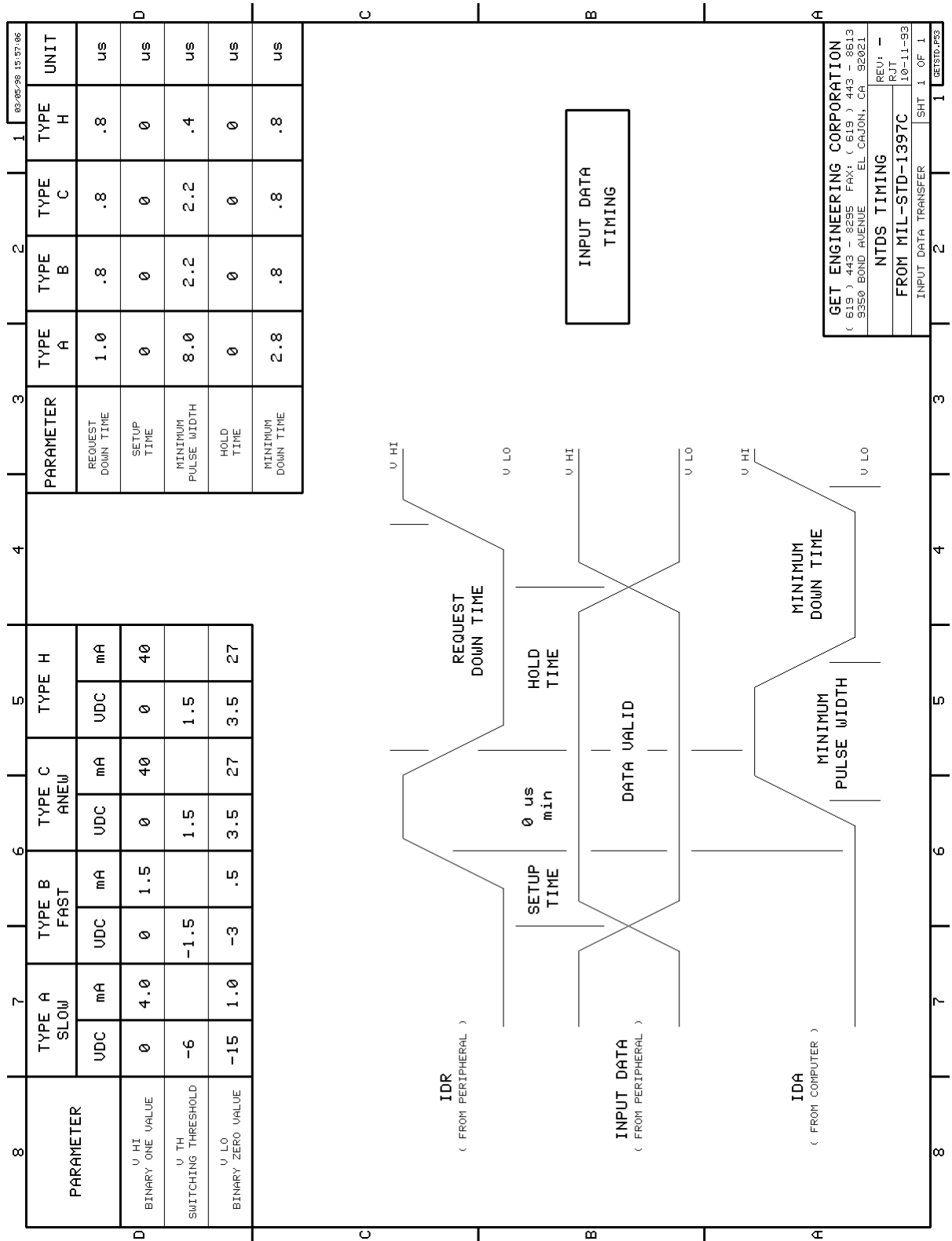
NTDS TIMING
 REV: -
 RJT

FROM MIL-STD-1397C 10-11-93

EXTERNAL FUNCTION TRANSFER | SHT 1 OF 1

FIGURE 1.3

INPUT DATA TIMING



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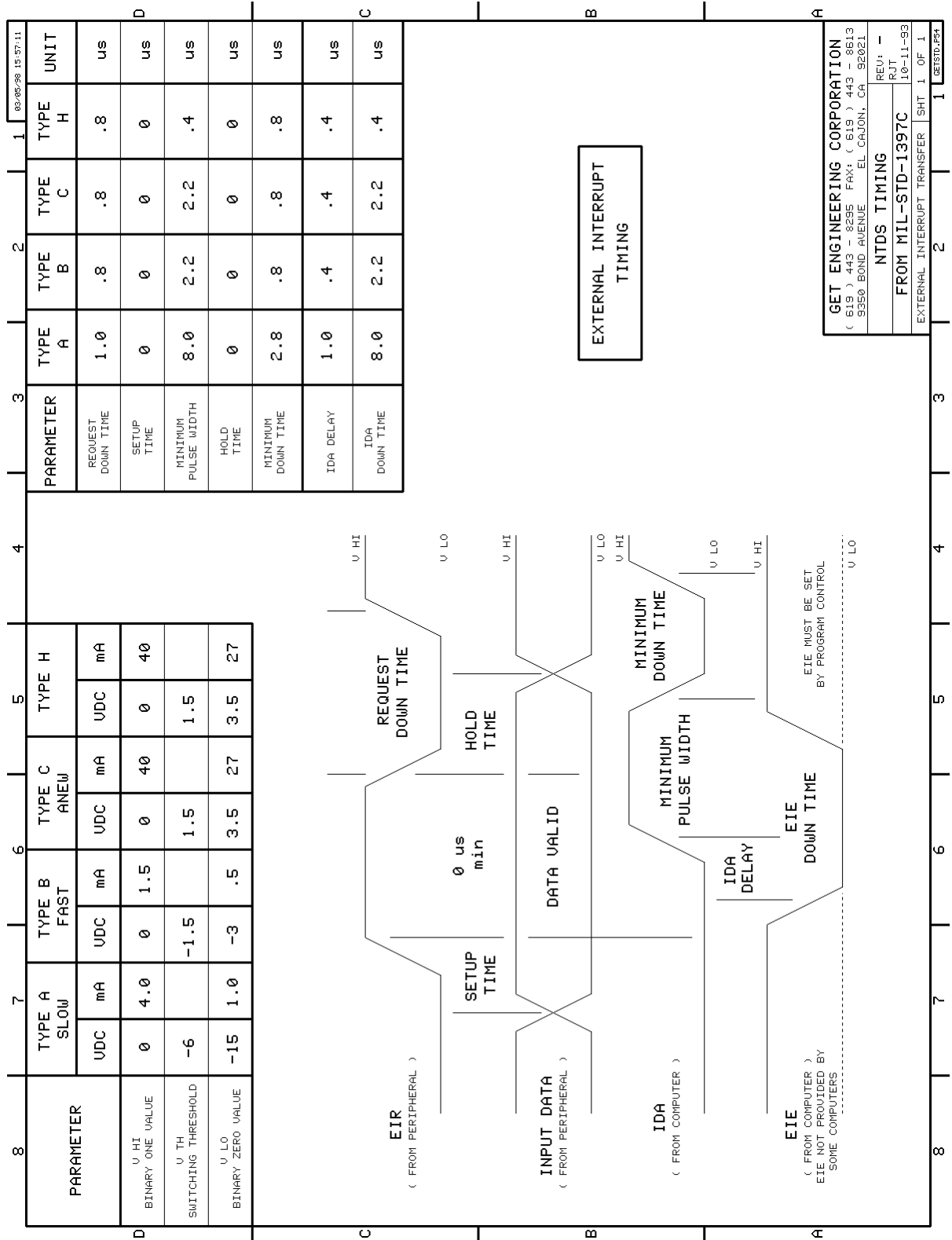
NTDS TIMING
 REV: -
 RJT

FROM MIL-STD-1397C
 10-11-93

INPUT DATA TRANSFER | SHT 1 OF 1 | GETSD.PDS

FIGURE 1.4

EXTERNAL INTERRUPT TIMING



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NTDS TIMING
 FROM MIL-STD-1397C
 REVISION: -
 DATE: 10-11-93

EXTERNAL INTERRUPT TRANSFER SHEET 1 OF 1
 GETSD.P54

FIGURE 1.5

PIPELINE MODE TIMING

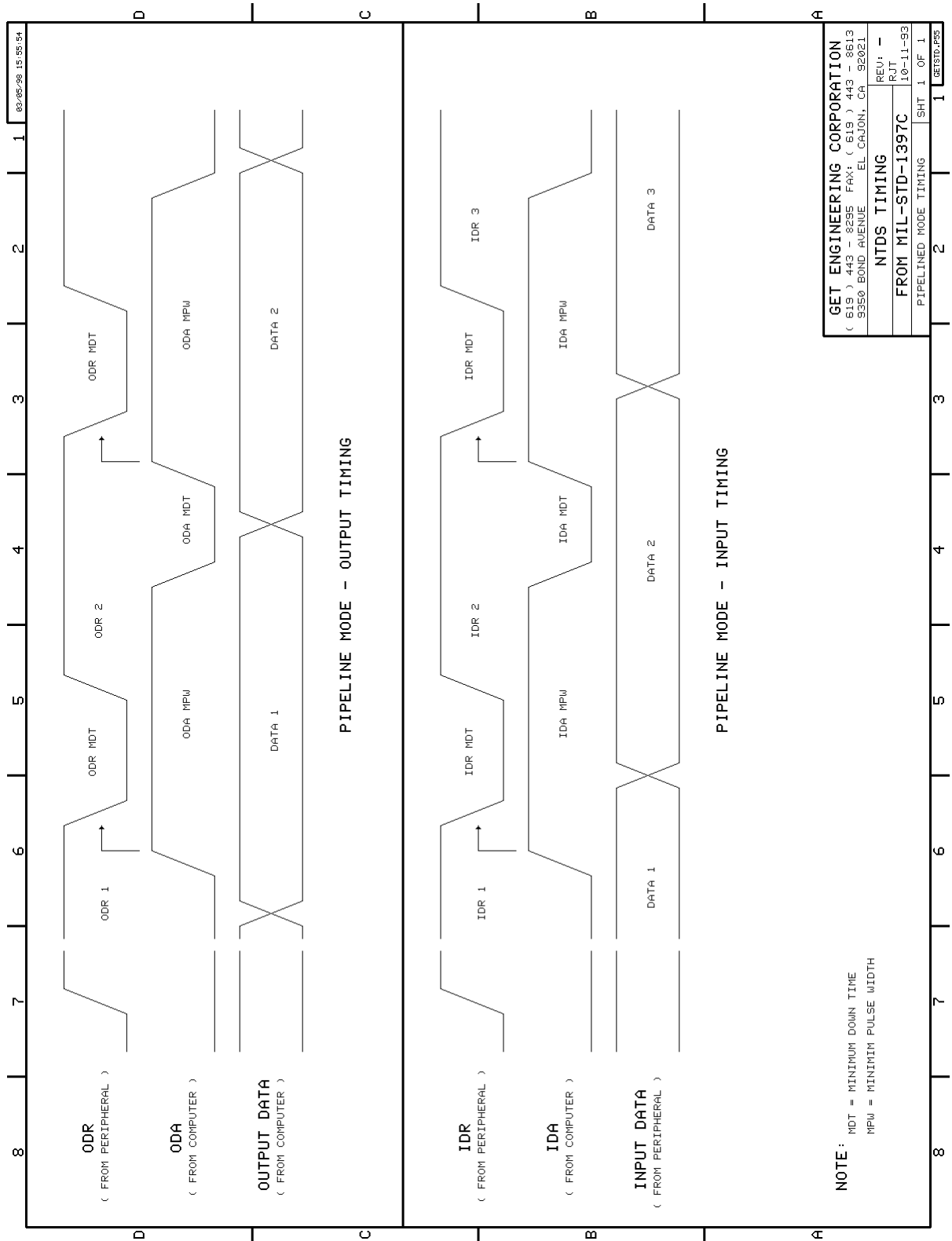


FIGURE 1.6

PULSED TIMING EXAMPLE

