GENERAL DISCUSSION
of the
MIL-STD-188/203-1A
(TADIL) A
ATDS SERIAL INTERFACE

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1.1 SCOPE

This document contains information discussing the general design philosophy used in implementation of GET ATDS Serial Interface Adaptors. This document is intended to assist qualified personnel in the development, operation, installation, and diagnosis of these adaptors. It is not the intent or purpose of this document to define the actual uses or applications of ATDS interfaces. Programming and application examples or outlines and diagrams which may be found in this document are intended only to illustrate the operation of the ATDS interface.

1.2 ATDS SERIAL OVERVIEW

The following is a brief operational description of a typical ATDS channel. It is intended as an aid in explaining the operation of a typical ATDS channel and as such does not cover all aspects of the communication protocol. Refer to MIL-STD-188-203-1A (Appendix D2) Military Standard Document for a complete description of ATDS data exchange protocols.

1.3 SERIAL TRANSFERS

Transfers of information between ATDS Data Terminal Sets (DTS) and Tactical Data System (TDS) Computers are accomplished in a complex half duplex mode. Three transfer operations are used: DTS to TDS data, TDS to DTS data, and TDS to DTS Address transfers.

1.3.1 DTS TO TDS DATA TRANSFERS

Data transfers from the DTS to the TDS computer are performed using the Frame, Data Clock, Incoming Data, and Outgoing Data Lines, as shown in Figure 1.1. The DTS generates a pulse on the Frame line when it desires to transmit a data frame to the TDS computer. When the computer is ready to receive, it issues a series of 26 pulses on the Data Clock Line to shift the serial data on the Incoming Data Line from the DTS to the computer. After a minimum delay of 7 microseconds the computer generates a second series of 26 clock pulses which resends the same serial data from the DTS to the computer again. The computer then compares the two received data words and, if they are not identical, generates a fault pulse on the Outgoing Data Line.

1.3.2 TDS TO DTS DATA TRANSFERS

Data transfers from the TDS computer to the DTS are performed using the Frame, Data Clock, Incoming Data, and Outgoing Data Lines, as illustrated in Figure 1.2. The DTS generates a pulse on the Frame line when it desires to receive a data frame from the TDS computer. When the computer is ready to transmit, it issues a series of 26 pulses on the Data Clock Line to shift the serial data on the Outgoing Data Line from the computer to the DTS. After a minimum delay of 7 microseconds the computer generates a second series of 26 clock pulses which returns the serial data just received from the computer back to the computer. The computer then compares the two received data words and, if they are not identical, generates a fault pulse on the Outgoing Data Line.

1.3.3 TDS TO DTS ADDRESS TRANSFERS

Address Frame transfers from the Tactical Data System computer to the DTS are performed using the Frame, Incoming Data, and Address Data, and Address Clock Lines, as illustrated in Figure 1.3. When the DTS desires to receive an address frame from the TDS computer it generates a simultaneous pulse on the Frame and Incoming Data lines. When the computer is ready to transmit, it issues a series of 7 pulses on the Address Clock Line to shift the serial data on the Address Data Line from the computer to the DTS.

1.3.4 DTS TO TDS DATA FORMAT

The 26 bit DTS to TDS serial data frame consists of two leading Control Bits (C1 and C2) followed by 24 Data Bits. The Control bits are used to indicate the quality of the received data. Control Bit C1 is generally used to indicate the presence of detected errors in the data field. Control Bit C2 is used as the frame start indication. This bit is SET in the first frame and CLEAR for all subsequent frames of each message.

1.3.5 DTS TO TDS ADDRESS FORMAT

The 7 bit DTS to TDS serial address frame consists of 6 leading Address Bits followed by a single Message Control Bit. The Message Control bit is typically used to define the message format to be used by the DTS during transmission.

1.3.6 TDS TO DTS DATA FORMAT

The 26 bit TDS to DTS serial data frame consists of two leading Control Bits (C1 and C2) followed by 24 Data Bits. The Control bits are used to indicate the type of the transmitted data. The data frame is valid when Control Bits C1 and C2 are both SET. A stop condition is indicated when either C1 or C2 are CLEAR. In this case the DTS will typically discard the data portion of the frame and transmit a special stop code.

1.4 SIDETONE INTERFACE OPERATION

The Sidetone Frame, Sidetone Data, and Sidetone Clock lines are used for test and data validation purposes. The Sidetone Interface provides an additional echo data path that returns to the TDS computer the data that was transmitted by the DTS.

1.4.1 DTS TO TDS SIDETONE TRANSFER

The 26 bit TDS to DTS serial data frame consists of two leading Control Bits followed by 24 Data Bits. The Sidetone transfers from the DTS to the TDS computer are performed using the Sidetone Frame, Sidetone Data, and Sidetone Data Clock, as shown in Figure 1.4. The DTS generates a pulse on the Sidetone Frame line when it desires to transmit a Sidetone Data frame to the TDS computer. When the computer is ready to receive, it issues a series of 26 pulses on the Sidetone Clock Line to shift the serial data on the Sidetone Data Line from the DTS to the computer. The computer then uses the received Sidetone Data to evaluate the transmission performance of the DTS.

1.5 ELECTRICAL CHARACTERISTICS

The signal interface lines between the TDS computer and the DTS are measured across a 100 Ohm load on the secondary winding of a terminating transformer. The amplitude of all pulses is -6 VDC, with respect to ground. This voltage is 0.0 VDC when no pulses are present. The width of the pulses from the TDS to the DTS is 200 nanosec. The width of the pulses from the DTS to the TDS is 600 nanosec. The nontatical interface (sidetone) lines have open collector drivers with the capability of sinking 20 mA to ground. The amplitude of the sidetone signals is nominally +5 VDC, with respect to ground. The sidetone receiver switching threshold is 1.5 VDC.

FIGURE 1.1

DTS TO TDS DATA FRAME TIMING

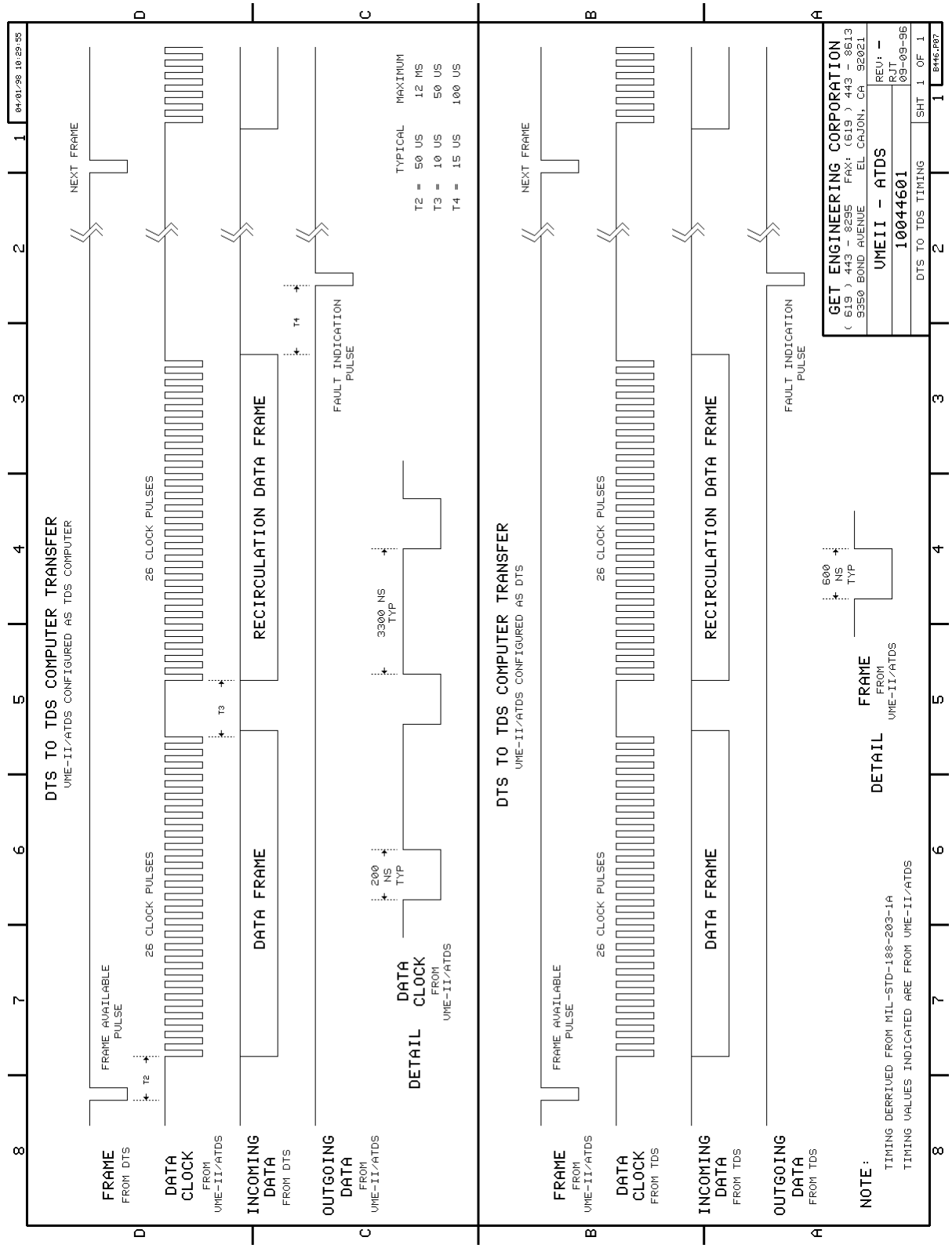

FIGURE 1.2

TDS TO DTS DATA FRAME TIMING

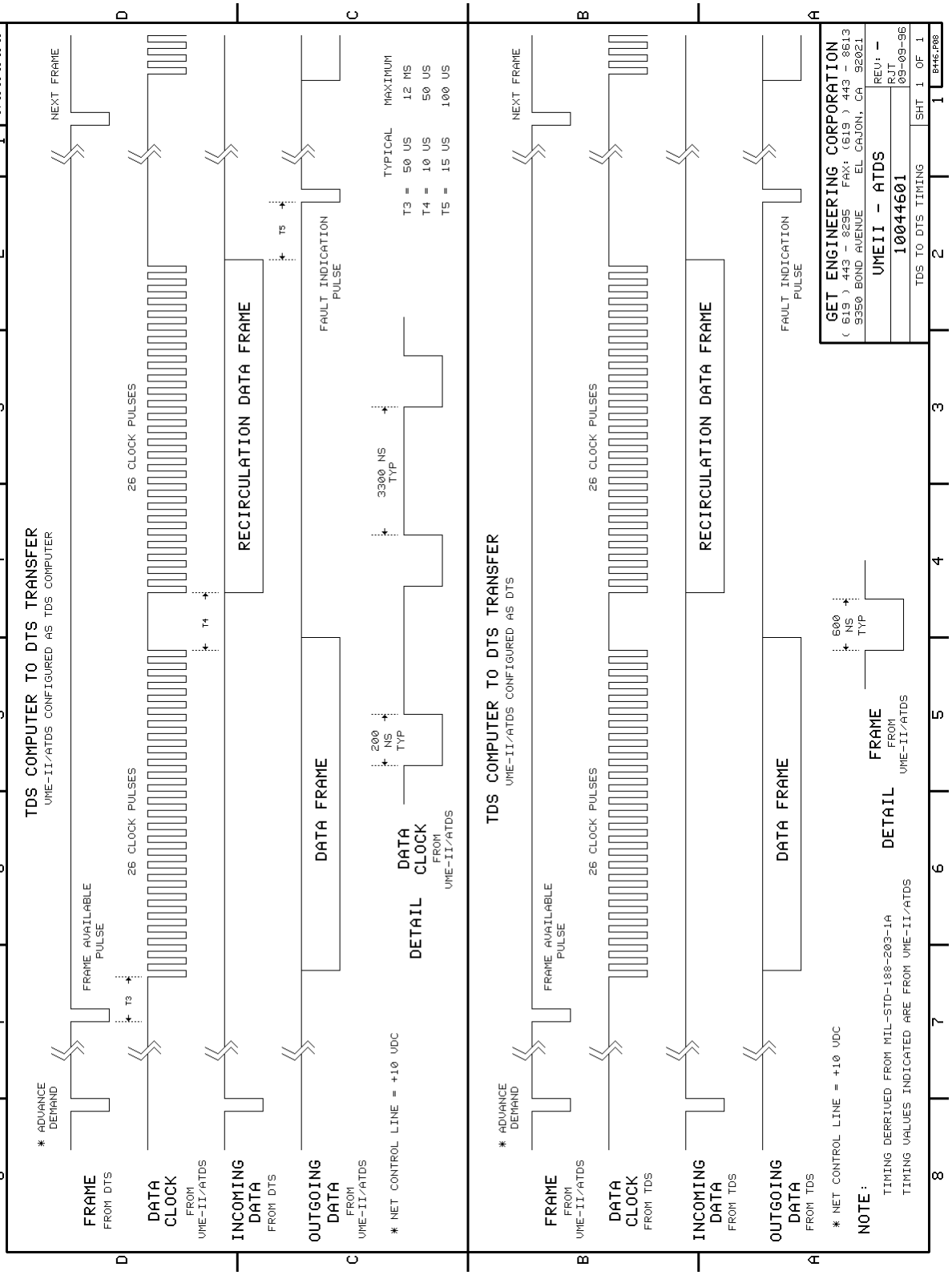

FIGURE 1.3

ADDRESS FRAME TIMING

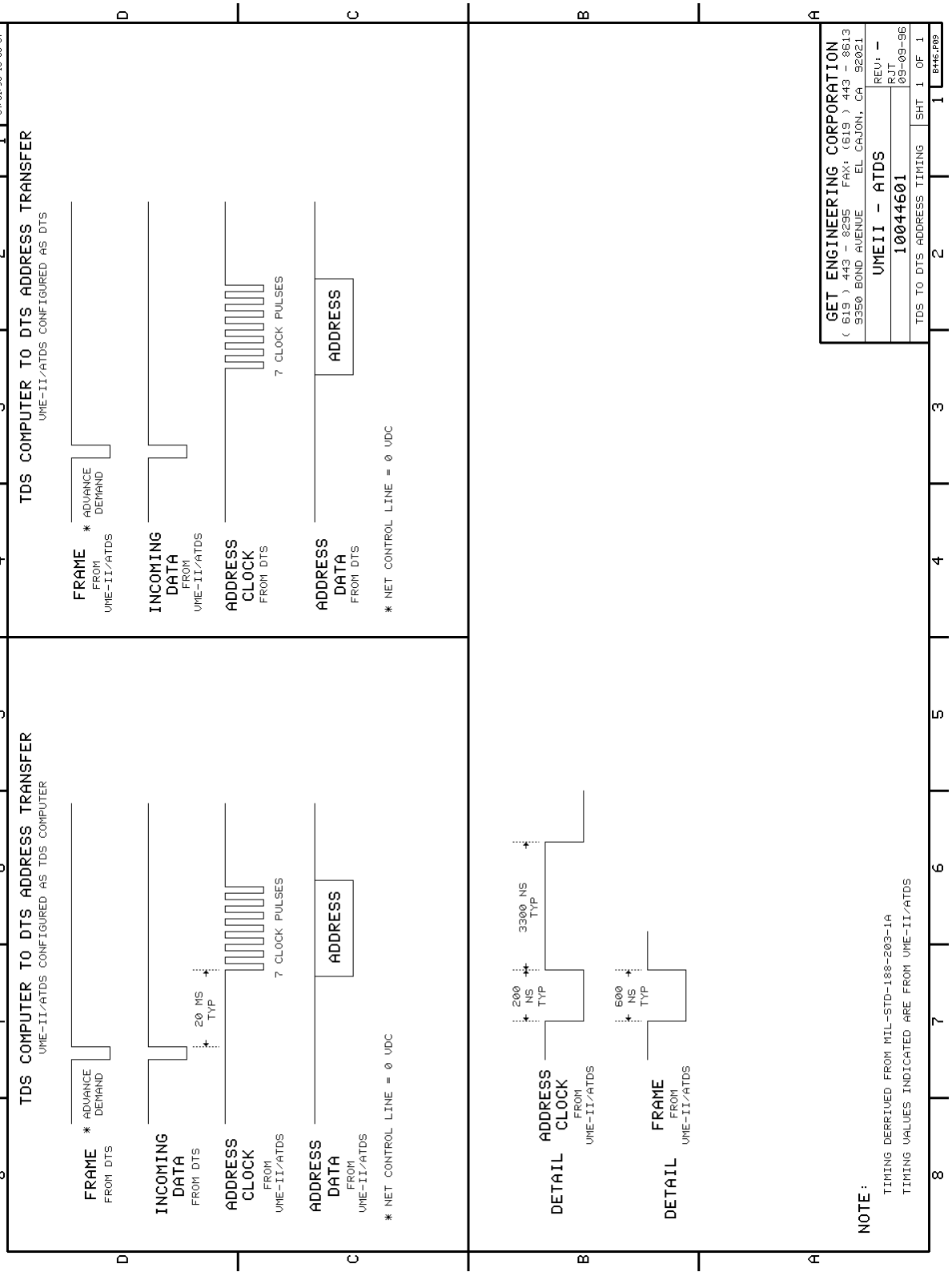

FIGURE 1.4

SIDETONE FRAME TIMING