I105

GET Engineering Corporation
NTDS Interface Adaptor Specialists

A GENERAL DISCUSSION
of the

MIL-STD-1397C (NAVY)

NTDS INTERFACE STANDARD

and the

MIL-STD-188-203-1A (D2)

ATDS SERIAL INTERFACE STANDARD

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* * NOTICE * *

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INTRODUCTION

1.1 THE NAVY TACTICAL DATA SYSTEM

The Navy Tactical Data System (NTDS) is based on the interaction of humans and machines. The NTDS helps coordinate fleet air defense, antisubmarine warfare, and surface defense operations. Through automation, the NTDS provides commanders with a broad picture of the current tactical situation and assists in directing operations in time to intercept potential enemy threats. The use of digital computers and digital data processing techniques reduces reaction time and increases force effectiveness.

1.2 A BRIEF HISTORY

In the later stages of World War II the Japanese began to abandon coordinated tight formation air attacks in favor of massed combined suicide and conventional attacks coming from all directions. These tactics created overwhelming amounts of lookout and radar tactical data that had to be processed manually in real time by the ships’ air defense coordinators. These tasks involved interpretation of radar data, identifying threats, relaying messages, and manually plotting the information on large plexiglass map display boards.

1.2.1 THE PROBLEM

During close range combat, the shipboard combat information center (CIC) is involved in complex tactical situations requiring important decisions to be made in a short period of time. The speed at which these combat situations must be solved is inconceivable to someone thinking in terms of typical human based CIC operations of the 1940’s. At times the sheer quantity of tactical data and reporting task complexity would overwhelm the plot crew causing data critical to the fleet defense to be late or lost.

1.2.2 THE SOLUTION

After performing task force battle assessments in the late 1940’s the Navy realized that it needed some new technology teamed with radar to help human users assimilate and interpret the massive amount of tactical data available from its new electronic radar and sonar sensor suites. The Navy Tactical Data System was conceived as an automated tool for assisting combat situation commanders in making rapid tactical decisions.

1.3 NTDS SYSTEM COMPONENTS

The NTDS consists of high-speed computers, data display consoles, communication links, and operational computer programs. The total system functions to collect, analyze, and correlate sensor data to obtain a clear picture of the tactical situation. A good tactical picture includes complete target data on all ships, aircraft, and submarines in the area of concern. This picture is then converted to digital format and supplied to the weapon systems of the ship and to other ships over the communications data link. Figure 1.1 shows the NTDS equipment grouping and how it interfaces with the weapons and ship sensor systems.

FIGURE 1.1

THE NTDS SYSTEM

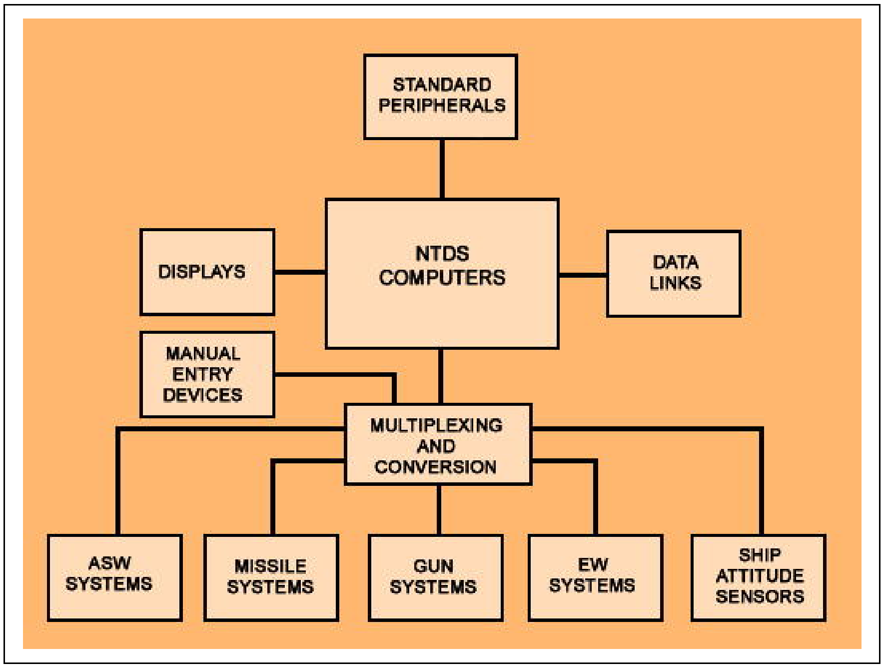
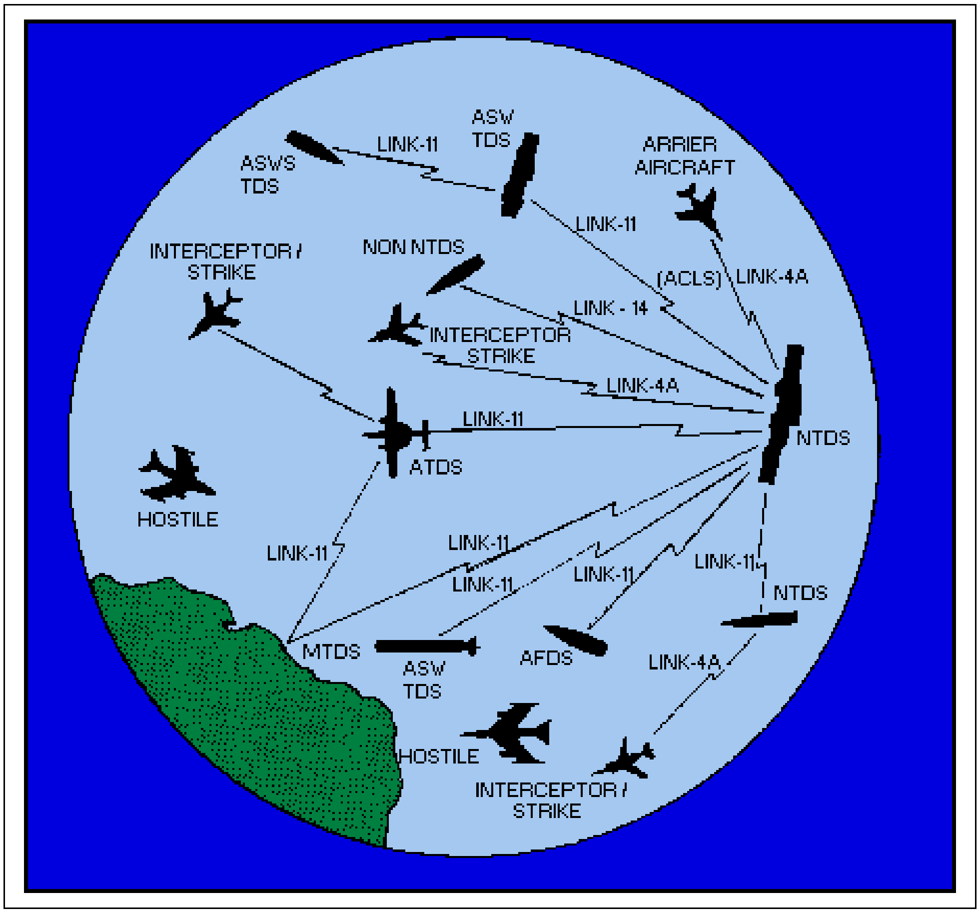


FIGURE 1.2

THE LINKS



1.3.1 NTDS COMPUTERS

The first production NTDS suite was the AN/USQ-20(V) and consisted of an assemblage of peripheral equipment and computers, designated the CP-642. In 1959 the navy specified a tactical computer design which would be modular, powerful, and reliable. Thus the CP-642 with 30 bit instructions, fourteen 30 bit I/O channels, and 32k word memory was born. The first CP-642 was delivered in 1960 and production continued until 1975 for a total of 380 computers.

1.3.1.1 EQUIPMENT STANDARDIZATION

As part of the standardization strategy the Navy defined the physical and electrical interface between the various equipment in the AN/USQ-20(V) suite. This specification came to be MIL-STD-1397C (NAVY) Military Standard Document and defines several parallel and serial equipment interface types. The standardization equipment interface strategy proved so successful that it was adapted for use by the navies of many other countries. GET produces interface adaptor and emulation products that enable non-NTDS equipped computers and peripheral equipment to comply with these Navy standards.

1.3.2 COMMUNICATIONS SUBSYSTEM

NTDS uses three separate data transmission links to maintain tactical data communications between tactical units (Figure 1.2). Each link is able to transfer data to other ships, aircraft, and shore facilities without the delay of human interface. The data processing subsystem formats the messages for each of the data links. These messages are based on shipboard inputs from displays, sensors, and other data links.

1.3.2.1 LINK 11

Link 11 (TADIL A) is a secure link between NTDS-equipped surface ships. Link 11 provides high-speed, computer-to-computer transfer of tactical information, command orders, and unit status to all tactical data systems. The type of tactical information transferred is surface, subsurface, air, and track information and consists of friendly, hostile, and unknown identity tracks. The new Link-11/22, a member of the Joint Message Standard (TADIL-J) family, will improve Link-11 connectivity and reliability and will be the common data link for all Navy and allied ships not equipped with Link-16.

1.3.2.2 LINK 14

Link 14 provides a means of transmitting track information to those units not capable of participating in the Link 11 network. Instead of being displayed automatically, the information is presented in a Teletype format and must be manually plotted.

1.3.2.3 LINK 4A

Link 4A is a secure data link between surface units and aircraft and permits the computer to take control of the autopilot in an equipped aircraft. It may control a flight out to a strike area and return it to base without the need for pilot action. The pilot also has the option of using his visual display to aid in understanding the intercept controller, or to totally ignore and override the link 4A transmission.

1.3.2.4 LINK 16

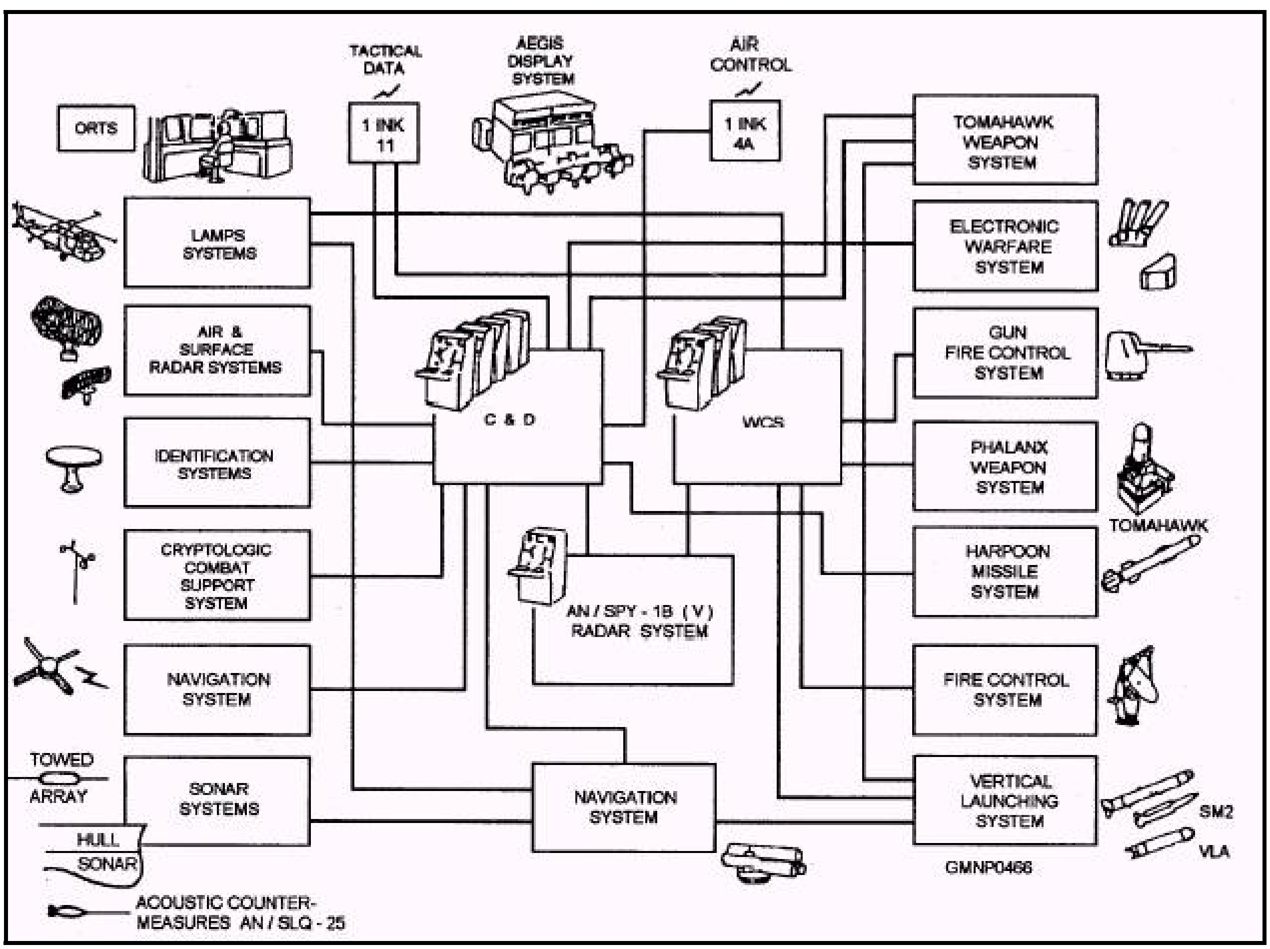
Link 16 (JTIDS/TADIL J) is a secure tactical data system with an embedded digital voice channel and Tactical Air Navigation (TACAN) functions. The high data rate JTIDS link provides aircraft and ships with crypto secure, jam-resistant, and low-probability of exploitation communications capability. This high capacity system provides a secure, jam resistant (via frequency hopping) link for voice communications, navigation, and tactical data, including secret information.

1.3.3 THE AEGIS SYSTEM

Over the years the NTDS has changed from a basic Combat Direction System (CDS) to the Advanced Combat Direction System (ACDS). The NTDS was originally considered an individual unit instead of a component of the combat system. The NTDS function is now being performed by the same equipment that performs other functions formerly not associated with NTDS. The AEGIS weapon system (Figure 1.3) is the first system designed under the one-system concept. The AEGIS Command and Decision (C&D) system not only performs the NTDS function but also controls the electronic warfare (EW) system, IFF challenges, and several other functions as well.

FIGURE 1.3

THE AEGIS COMBAT SYSTEM



SECTION 2
NTDS PARALLEL INTERFACE

2.1 SCOPE

The following discussion addresses the general design philosophy used in the design of GET NTDS Parallel Interface adaptors and supporting products and is intended to assist qualified personnel in their implementation and installation. It is not the intent or purpose of this document to define the actual uses or application of NTDS interface adaptors. Programming and application examples or diagrams which may be found in this document are intended only to illustrate the operation of the NTDS interface.

2.1.1 NTDS OVERVIEW

The NTDS interface was originally developed in the early 1960's as a standardized point to point communications specification to be used between all Navy tactical computers and their peripheral devices. Four types of Parallel and two types of Serial data format systems are specified. The physical connection between compatible equipment is by means of a pair of cables. One cable is used to transfer Input Data and Interrupts while the other cable transfers Output Data and Commands. The individual transfers are performed using a strict Request / Acknowledge timing protocol. The connector types, contact assignments, and cable types are specified. Actual data and command word formats, applications, and actions invoked by the transactions are not addressed by the specification.

2.2 NTDS PARALLEL INTERFACE OVERVIEW

The GET NTDS Parallel Interface Adaptors can be configured to operate as NTDS Peripheral or Computer channel devices. Each CHANNEL consists of an Input PORT and an Output PORT, each containing up to 32 data lines and four control lines (Figure 2.2). The transfer of information by each port is conducted using these control lines. The following discussion is intended only as an aid in explaining a general operation of an NTDS Parallel Data channel and does not cover all aspects of the NTDS protocol. For a complete description of the NTDS protocols refer to MIL-STD-1397C (NAVY) Military Standard Document.

2.2.1 PARALLEL INTERFACES

There are four types of NTDS Parallel interfaces specified, each of which can operate in three Categories. The NTDS TYPE defines the electrical interface characteristics while the CATEGORY describes the signal timing protocol used for information exchange operations.

2.2.2 PARALLEL INTERFACE CATEGORIES

The GET NTDS parallel interface ports are individually configurable to operate as Computer or Peripheral channels. This enables a single interface adaptor to operate in any one of the three NTDS equipment categories defined in MIL-STD-1397C. These equipment categories are:

A. Category I - Computer to Peripheral
B. Category II - Computer to Computer (Inter-Computer)
C. Category III - Peripheral to Peripheral (Inter-Peripheral)

2.2.3 PARALLEL INTERFACE CATEGORY CONFIGURATION

In Category II mode the Output port operates as a Peripheral device and the Input port operates as a Computer. In Category III mode the Output port operates as a Computer and the Input port operates as a Peripheral device. In the Passive Monitor mode the Output port is placed in the tristate mode and the Input port records the transfers between two other NTDS devices. Additionally, the Computer interfaces can be configured to operate with either interlocked or pulsed signal timing.

2.2.4 PARALLEL INTERFACE TIMING

The state (logic 1 or 0) of the NTDS Data lines is determined by their DC voltage level, and do not have to be cleared between successive transactions. The only restriction is that the Data lines must be stable during that time that the associated control line indicates validity. The control signals are edge significant and the receiving device must be able to recognize their change of state (from logic 1 to 0 or 0 to 1). The receiving device must not recognize a subsequent logic 1 until that line first transitions to the logic 0 state.

2.2.5 PARALLEL INTERFACE TYPES

Parallel interface channels can be configured to operate in NTDS TYPE A (SLOW), TYPE B (FAST), TYPE C (ANEW), or TYPE H (HIGH THROUGHPUT) environments. A special TRISTATE (OPEN CABLE) mode is also provided. Figure 2.1 illustrates the required electrical connection schemes for each type.

2.2.5.1 TYPE A (SLOW)

The Type A mode, also called SLOW, supports transfer rates of 41.67 K words per second on one cable. Nominal voltage levels of 0.0 VDC (logic 1), -15 VDC (logic 0), and switching thresholds of -6 VDC are used. Controlled slew rate driver outputs with linear characteristics are required. The single ended receiver circuits must be able to reject input transient pulse signals with specific maximum energy levels (30 Vμs). The receiver outputs must be logic 0 for open input conditions. Maximum specified cable lengths are 300 ft.

2.2.5.2 TYPE B (FAST)

In Type B mode, also called FAST, transfer rates of 250 K words per second on one cable are possible. Nominal voltage levels of 0.0 VDC (logic 1), -3 VDC (logic 0), and switching thresholds of -1.5 VDC are used. The referenced input receiver circuits must reject large common mode input transient pulses or DC signals (+/- 7.5 VDC). The receiver outputs must be logic 0 for all open input conditions. Controlled slew rate driver outputs are required. Depending on cable type used, maximum specified cable lengths are 50 or 100 ft.

2.2.5.3 TYPE C (ANEW)

The Type C mode, also called ANEW, supports transfer rates of 250 K words per second on one cable. Nominal voltage levels of 0.0 VDC (logic 1), +3.5 VDC (logic 0), and thresholds of +1.5 VDC are used. The referenced input receivers must reject large common mode input transient pulses or DC signals (+/-6 VDC). The receiver outputs must be logic 0 for all open input conditions. Controlled slew rate driver outputs are required. Depending on cable type used, maximum specified cable lengths are 100 or 250 ft.

2.2.5.4 TYPE H (HIGH THROUGHPUT)

In Type H mode, also called HIGH THROUGHPUT or FAST ANEW, transfer rates of 500 K words per second on one cable are possible. Nominal voltage levels of 0.0 VDC (logic 1), +3.5 VDC (logic 0), and thresholds of +1.5 VDC are used. The referenced input receivers must reject common mode input transient pulse or DC signals (+/- 6 VDC). The receiver outputs must be logic 0 for all open input conditions. Controlled slew rate driver outputs are required. Depending on cable type used, maximum specified cable lengths are 100 or 250 ft.

2.2.5.5 DRIVER TRISTATE (OPEN CABLE)

To allow for bussed configurations, hot spares, connection errors, and other unanticipated connection configurations, while the tristate mode is selected the NTDS outputs shall not be damaged nor shall they present less than 100,000 ohms impedance when they are driven by an externally connected signal source. When the tristate mode is selected the NTDS outputs will not be damaged by voltage excursions that are within the range of plus 10 volts to minus 18 volts with respect to the driver signal return connection.

2.2.5.6 ADDITIONAL RECEIVER CHARACTERISTICS

The NTDS inputs shall not be damaged by voltage excursions that are in the range of 15 VDC to minus 24 VDC, with respect to the signal return connection. When the inputs are driven beyond the maximum operating limits they may temporarily sink or source more current than specified. The output of the receiver shall not switch as a result of any input signal that has an amplitude between plus 7.5 VDC to minus 17.5 VDC if the duration and amplitude are common to the input and the return connection (common mode).

2.3 CATEGORY I OUTPUT PORT OPERATION

Transfer of information between NTDS computers and peripherals is accomplished using two methods: Data and Functions. The Output Port transactions are controlled by the Peripheral's request lines and the Computer's acknowledge lines.

2.3.1 OUTPUT DATA TIMING

A peripheral device sets its Output Data Request (ODR) line when it is in a condition to accept an Output Data (OD) word from the NTDS computer. The computer responds, at its convenience, by activating its Output Data Acknowledge (ODA) line. The active ODA line indicates to the peripheral device that the data contained on the OD lines is valid and should be sampled. The peripheral device acknowledges the receipt of data by deactivating its ODR line. The signal timing relationships for Output Data transfers are shown in Figure 2.3.

2.3.2 EXTERNAL FUNCTION TIMING

A peripheral device sets its External Function Request (EFR) line when it is in a condition to accept an External Function (EF) command word from the NTDS computer. The computer responds, at its convenience, by activating its External Function Acknowledge (EFA) line. The active EFA line indicates to the peripheral device that the command word contained on the OD lines is valid and should be sampled. The peripheral device acknowledges the receipt of data by deactivating its EFR line. Figure 2.4 illustrates External Function timing.

2.3.2.1 FORCED EXTERNAL FUNCTION TIMING

Some NTDS computers have the ability of sending External Functions with Force. These transfers require no request (EFR) from the peripheral device. The computer, at its convenience, activates its External Function Acknowledge (EFA) line, indicating to the peripheral device that the command word contained on the OD lines is valid and should be sampled. The EFR line is not monitored during the Forced EF. The peripheral device has no control over the rate at which Forced EFs are sent.

2.4 CATEGORY I INPUT PORT OPERATION

Transfer of information between NTDS computers and peripherals is accomplished in two major methods: Data and Interrupts. The Input Port transactions are controlled by the Peripheral's request lines and the Computer's Input Acknowledge and Interrupt Enable lines. Only one of the peripheral's request lines line may be active at any one time.

2.4.1 INPUT DATA TIMING

An active Input Data Request (IDR) indicates to the computer that the peripheral has placed valid data on the data lines. The Computer’s Input Data Acknowledge (IDA) line indicates to the peripheral that it has sampled this data. When the peripheral device senses that the IDA line is active it deactivates its IDR line. When the computer deactivates its IDA line the input cycle is complete. Figure 2.5 illustrates Input Port control signal timing.

2.4.2 EXTERNAL INTERRUPT TIMING

Transmission of External Interrupt words from the peripheral device to the computer is controlled by the External Interrupt Enable (EIE) line. When sending an External Interrupt the peripheral activates its External Interrupt Request (EIR) line indicating the validity of the interrupt data on the data lines. At its convenience the computer accepts the interrupt code, deactivates its EIE line and activates its IDA line. The peripheral device senses that the IDA line is active and responds by deactivating its EIR line. When the computer deactivates its IDA line the input cycle is complete. That not all computers have an EIE line and peripheral equipment may be designed to initiate an External Interrupt transfer without monitoring the EIE line. This does not, however, alter the timing sequence since the computer will still accept the interrupt at its own convenience using the IDA line. Refer to Figure 2.6.

2.5 NTDS CHANNEL IMPLEMENTATION

The MIL-STD-1397C (NAVY) Specification allows a wide variation in the implementation of NTDS channel interface design architectures. This allows the designer to develop circuits which maximize total system channel throughput. The GET NTDS channels are designed to take full advantage of these modes. The three main design schemes currently used are:

A. Interlocked
B. Pipeline
C. Pulse

2.5.1 INTERLOCKED OPERATION

In Interlocked timing, the most fundamental transaction protocol, the peripheral device will not initiate a subsequent transaction until the current transaction has completely finished. The NTDS timing specifications still allow the channel to operate at full transfer rates as long as the peripheral device does not extend any active request lines beyond the minimum required time.

2.5.1.1 INTERLOCKED OUTPUT TIMING

A peripheral device sets its Request (ODR or EFR) lines when it is in a condition to accept an Output from the computer. The computer responds, at its convenience, by activating its Output Acknowledge line (ODA or EFA), indicating that the data is valid. The peripheral then samples the data and may deactivate its Request line any time after that. The computer maintains its acknowledge line active until the minimum pulse width period has expired or, if the peripheral device has not yet deactivated the Request line, until the request line is deactivated (whichever comes last). The Output cycle is completed when the computer deactivates its acknowledge line. Figures 2.3 and 2.4 illustrate the Output Port signal timing.

2.5.1.2 INTERLOCKED INPUT TIMING

When the peripheral device wishes to send information to the computer it places the associated data on the data lines and activates an Input Request (IDR or EIR). The computer samples the data lines and activates the Input Data Acknowledge (IDA). The peripheral device may deactivate its request line at any time after sensing that the IDA line has been activated. The computer continues to maintain its IDA line active until the minimum pulse width time has expired or, if the peripheral device has not yet deactivated the Input Request line, until the request line is deactivated (whichever comes last). When the computer deactivates its IDA line the input cycle is considered completed. Figures 2.5 and 2.6 illustrate the port Input control signal timing.

2.5.2 PIPELINE OPERATION

Pipelined timing (Figure 2.7) enables a channel to operate at maximum transfer rates by allowing the peripheral device to request the next transfer during the closing phase of the current transaction. This is possible because the request minimum low time can then be satisfied during the acknowledge minimum pulse width times, and then reactivated, requesting the next transfer before the initial acknowledge pulse period has expired. This feature allows the cable control line propagation delays to occur during the acknowledge pulse width and hold times, where they do not affect total system throughput.

2.5.2.1 PIPELINED OUTPUT TIMING

A peripheral device sets its Request (ODR or EFR) lines when it is ready to accept an Output. At it’s convenience, the computer responds by presenting valid data and activating the appropriate acknowledge line (ODA or EFA). The peripheral samples the data, deactivates its Request line, and starts a Request line inactive timer. The computer continues to maintain its acknowledge line active until its minimum pulse width time has expired. The peripheral device, after the minimum low time has been satisfied, reactivates the Request line, regardless of the state of the computer acknowledge line. When the computer deactivates its acknowledge line the current output cycle is complete, and if the request line has been reactivated, a new cycle can begin immediately.

2.5.2.2 PIPELINED INPUT TIMING

When the peripheral wishes to send information to the computer it places valid data on the data lines and activates an Input Request (IDR or EIR). The computer samples the data lines and activates the Input Data Acknowledge (IDA). When the peripheral device senses that the IDA line is active may deactivate its Request line, and start a Request line inactive timer. The computer continues to maintain its IDA line active until the minimum pulse width time has expired. The peripheral device, after its minimum low time has been satisfied, may present a new data word and reactivate the Input Request line, regardless of the state of the computer IDA line. When the computer deactivates its IDA line the current input cycle is complete, and if the request line has been reactivated, a new cycle can begin.

2.5.3 PULSED OPERATION

The pulsed operation can be used for both the interlocked and pipelined modes. In pulsed operation computer is designed to maintain its active acknowledge lines for only the minimum required period, regardless of the state of the corresponding peripheral request lines. Pulsed mode timing is illustrated in Figure 2.8.

2.5.3.1 PULSED OUTPUT TIMING

A peripheral device sets its Request (ODR or EFR) lines when it is in a condition to accept an Output from the NTDS computer. The computer responds by activating its Output Acknowledge line and maintaining it active until its minimum pulse width time has expired. The computer then deactivates the acknowledge line, regardless of the state of the request line. The peripheral device may deactivate its Request line at any time after the acknowledge line has been activated. The peripheral device can reactivate the Request line and start the next cycle only after its request line minimum low time.

2.5.3.2 PULSED INPUT TIMING

When the peripheral wishes to send information to the computer it activates an Input Request line (IDR or EIR). The computer samples the data lines and activates the Input Data Acknowledge (IDA), which remains active until the minimum pulse width time has expired. The computer then deactivates the acknowledge line, regardless of the state of the request line. The peripheral device may deactivate its Request line at any time after the IDA line has been activated. The peripheral device can reactivate the Request line and start the next cycle only after its request line minimum low time requirement has been met.

FIGURE 2.1

ELECTRICAL CONNECTIONS

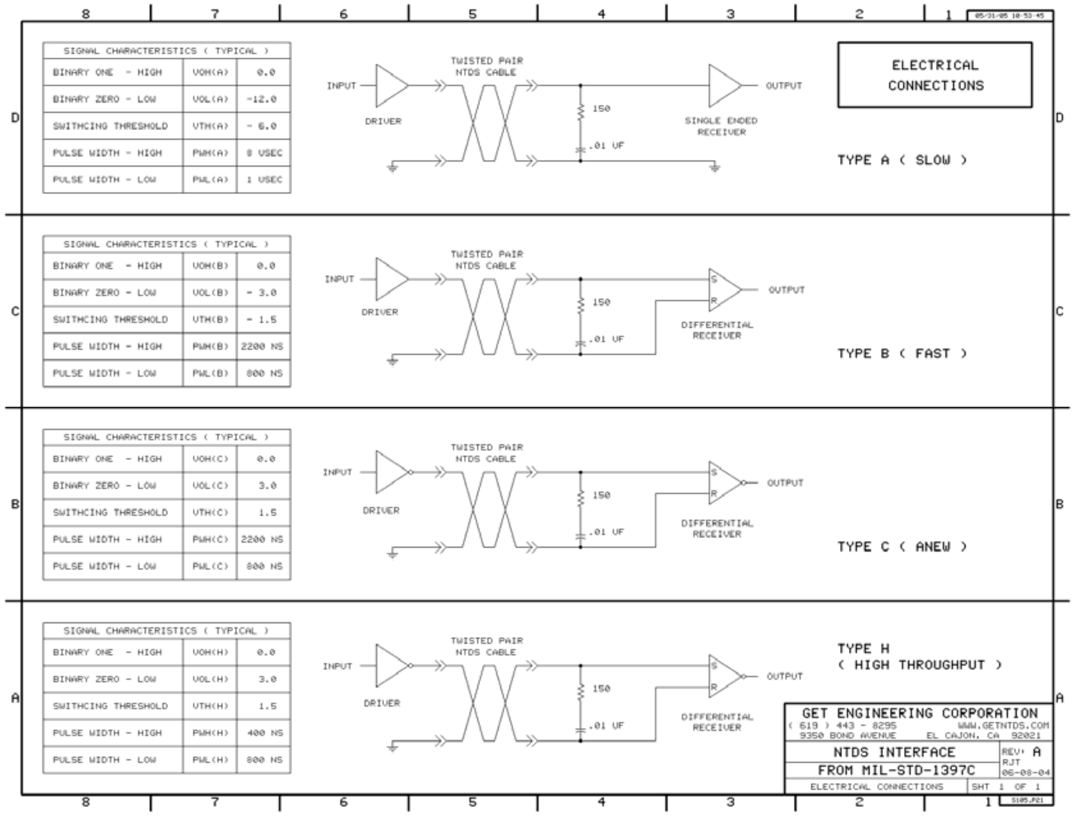


FIGURE 2.2

NTDS CHANNEL CONNECTIONS

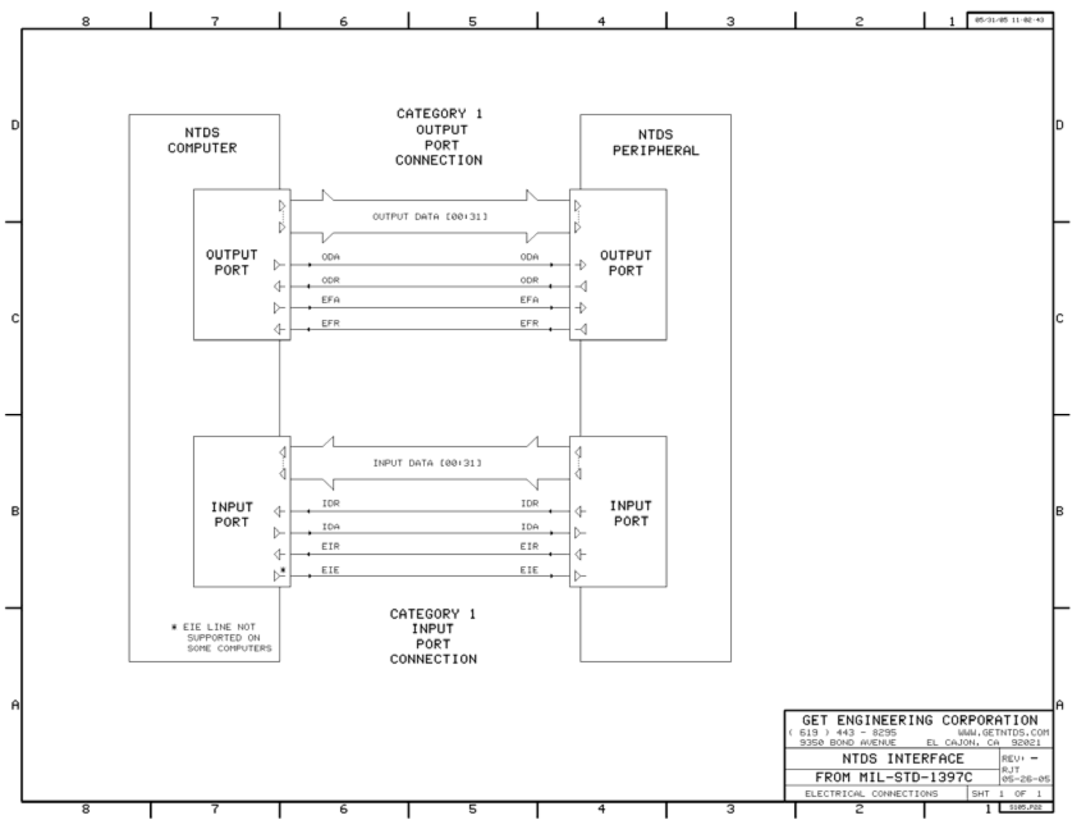
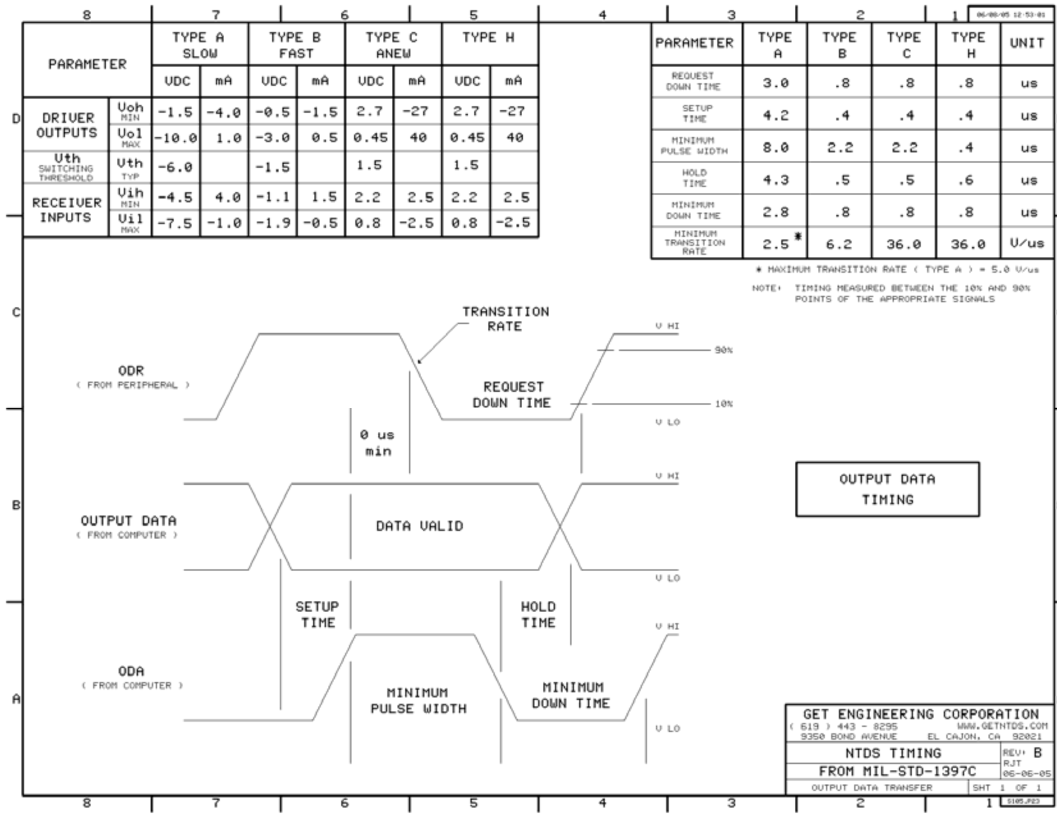


FIGURE 2.3

OUTPUT DATA TIMING

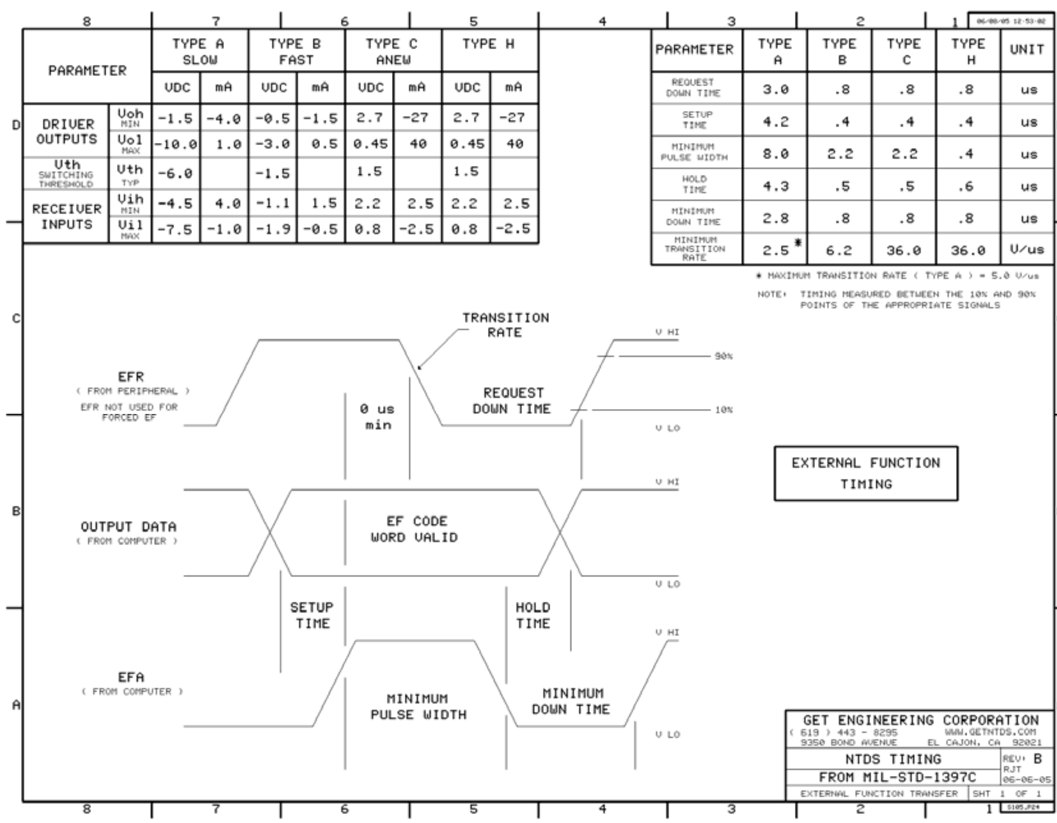


PARAMETER		TYPE A SLOW VDC	TYPE A SLOW mA	TYPE B FAST VDC	TYPE B FAST mA	TYPE C ANEW VDC	TYPE C ANEW mA	TYPE H VDC	TYPE H mA
DRIVER OUTPUTS	Voh MIN	-1.5	-4.0	-0.5	-1.5	2.7	-27	2.7	-27
	Vol MAX	-10.0	1.0	-3.0	0.5	0.45	40	0.45	40
Vth SWITCHING THRESHOLD	Vth TYP	-6.0		-1.5		1.5		1.5	
RECEIVER INPUTS	Vih MIN	-4.5	4.0	-1.1	1.5	2.2	2.5	2.2	2.5
	Vil MAX	-7.5	-1.0	-1.9	-0.5	0.8	-2.5	0.8	-2.5

PARAMETER	TYPE A	TYPE B	TYPE C	TYPE H	UNIT
REQUEST DOWN TIME	3.0	.8	.8	.8	us
SETUP TIME	4.2	.4	.4	.4	us
MINIMUM PULSE WIDTH	8.0	2.2	2.2	.4	us
HOLD TIME	4.3	.5	.5	.6	us
MINIMUM DOWN TIME	2.8	.8	.8	.8	us
MINIMUM TRANSITION RATE	2.5*	6.2	36.0	36.0	V/us

FIGURE 2.4

EXTERNAL FUNCTION TIMING

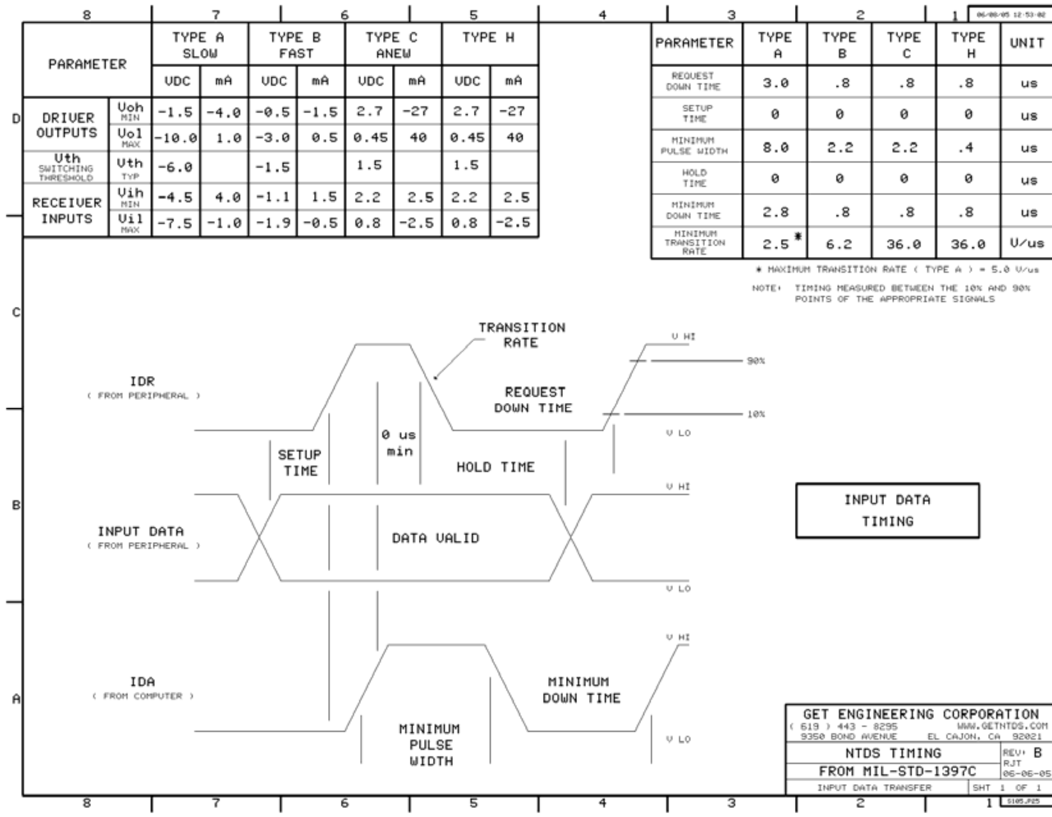


PARAMETER		TYPE A SLOW VDC	TYPE A SLOW mA	TYPE B FAST VDC	TYPE B FAST mA	TYPE C ANEW VDC	TYPE C ANEW mA	TYPE H VDC	TYPE H mA
DRIVER OUTPUTS	Voh MIN	-1.5	-4.0	-0.5	-1.5	2.7	-27	2.7	-27
	Vol MAX	-10.0	1.0	-3.0	0.5	0.45	40	0.45	40
Vth SWITCHING THRESHOLD	Vth TYP	-6.0		-1.5		1.5		1.5	
RECEIVER INPUTS	Vih MIN	-4.5	4.0	-1.1	1.5	2.2	2.5	2.2	2.5
	Vil MAX	-7.5	-1.0	-1.9	-0.5	0.8	-2.5	0.8	-2.5

PARAMETER	TYPE A	TYPE B	TYPE C	TYPE H	UNIT
REQUEST DOWN TIME	3.0	.8	.8	.8	us
SETUP TIME	4.2	.4	.4	.4	us
MINIMUM PULSE WIDTH	8.0	2.2	2.2	.4	us
HOLD TIME	4.3	.5	.5	.6	us
MINIMUM DOWN TIME	2.8	.8	.8	.8	us
MINIMUM TRANSITION RATE	2.5*	6.2	36.0	36.0	V/us

FIGURE 2.5

INPUT DATA TIMING

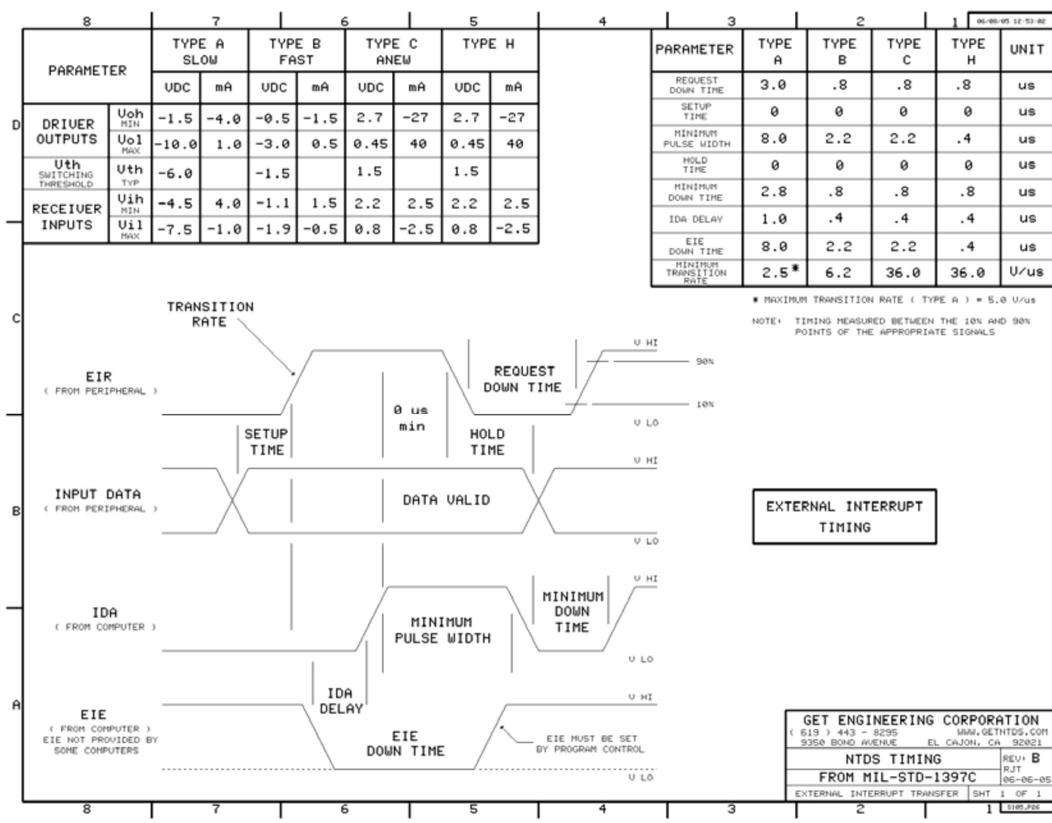


PARAMETER		TYPE A SLOW VDC	TYPE A SLOW mA	TYPE B FAST VDC	TYPE B FAST mA	TYPE C ANEW VDC	TYPE C ANEW mA	TYPE H VDC	TYPE H mA
DRIVER OUTPUTS	Voh MIN	-1.5	-4.0	-0.5	-1.5	2.7	-27	2.7	-27
DRIVER OUTPUTS	Vol MAX	-10.0	1.0	-3.0	0.5	0.45	40	0.45	40
Vth SWITCHING THRESHOLD	Vth TYP	-6.0		-1.5		1.5		1.5	
RECEIVER INPUTS	Vih MIN	-4.5	4.0	-1.1	1.5	2.2	2.5	2.2	2.5
RECEIVER INPUTS	Vil MAX	-7.5	-1.0	-1.9	-0.5	0.8	-2.5	0.8	-2.5

PARAMETER	TYPE A	TYPE B	TYPE C	TYPE H	UNIT
REQUEST DOWN TIME	3.0	.8	.8	.8	us
SETUP TIME	0	0	0	0	us
MINIMUM PULSE WIDTH	8.0	2.2	2.2	.4	us
HOLD TIME	0	0	0	0	us
MINIMUM DOWN TIME	2.8	.8	.8	.8	us
MINIMUM TRANSITION RATE	2.5*	6.2	36.0	36.0	V/us

FIGURE 2.6

EXTERNAL INTERRUPT TIMING



PARAMETER		TYPE A SLOW VDC	TYPE A SLOW mA	TYPE B FAST VDC	TYPE B FAST mA	TYPE C ANEW VDC	TYPE C ANEW mA	TYPE H VDC	TYPE H mA
DRIVER OUTPUTS	Voh MIN	-1.5	-4.0	-0.5	-1.5	2.7	-27	2.7	-27
DRIVER OUTPUTS	Vol MAX	-10.0	1.0	-3.0	0.5	0.45	40	0.45	40
Vth SWITCHING THRESHOLD	Vth TYP	-6.0		-1.5		1.5		1.5	
RECEIVER INPUTS	Vih MIN	-4.5	4.0	-1.1	1.5	2.2	2.5	2.2	2.5
RECEIVER INPUTS	Vil MAX	-7.5	-1.0	-1.9	-0.5	0.8	-2.5	0.8	-2.5

PARAMETER	TYPE A	TYPE B	TYPE C	TYPE H	UNIT
REQUEST DOWN TIME	3.0	.8	.8	.8	us
SETUP TIME	0	0	0	0	us
MINIMUM PULSE WIDTH	8.0	2.2	2.2	.4	us
HOLD TIME	0	0	0	0	us
MINIMUM DOWN TIME	2.8	.8	.8	.8	us
IDA DELAY	1.0	.4	.4	.4	us
EIE DOWN TIME	8.0	2.2	2.2	.4	us
MINIMUM TRANSITION RATE	2.5*	6.2	36.0	36.0	V/us

FIGURE 2.7

PIPELINE MODE TIMING

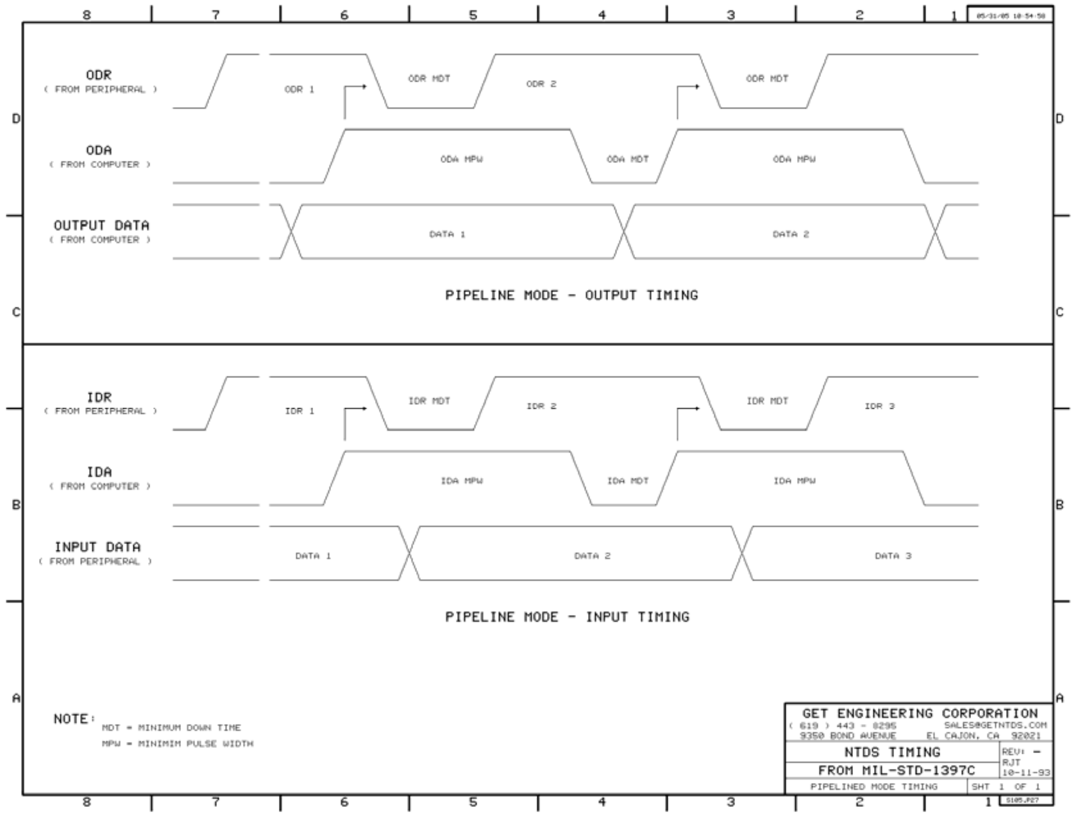
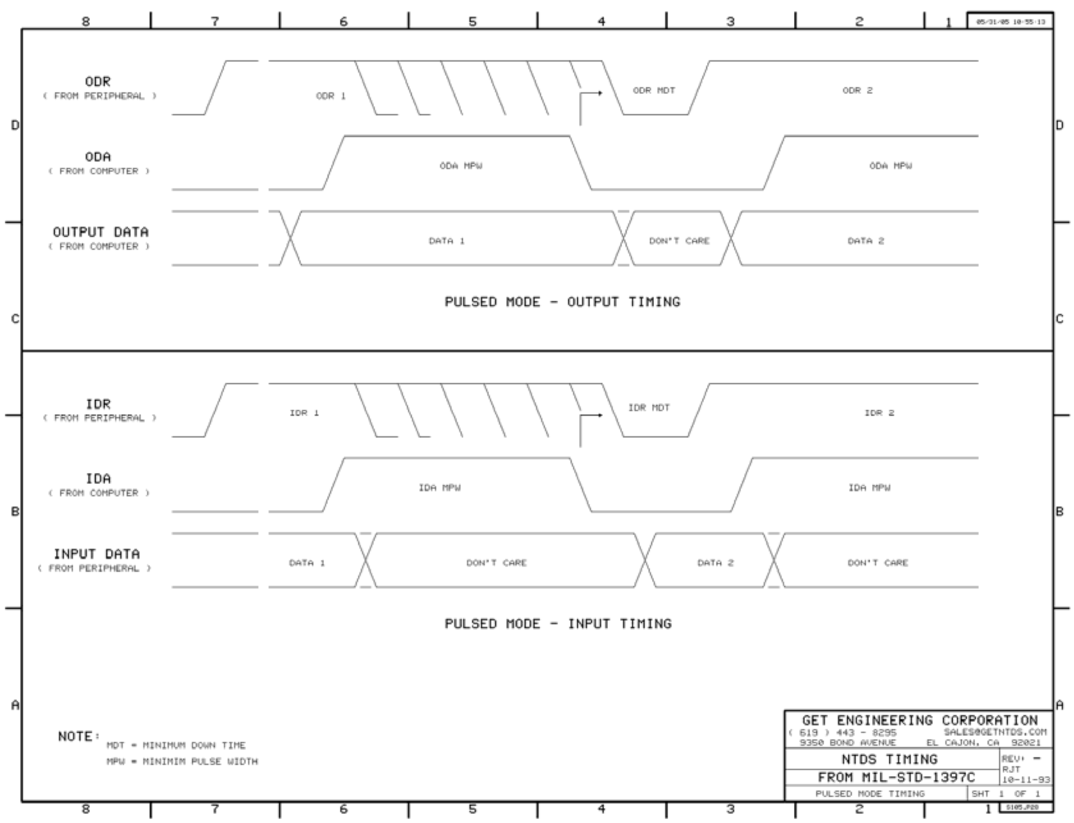


FIGURE 2.8

PULSED TIMING EXAMPLE



SECTION 3
NTDS TYPE D SERIAL INTERFACE

3.1 NTDS TYPE D SERIAL

The following discussion addresses the general design philosophy used in the design of GET NTDS Type D Serial Interface adaptors and supporting products. This discussion is intended as an aid in explaining a general operation of an NTDS Type D channel and does not cover all protocol aspects. For a complete protocol description refer to MIL-STD-1397C (NAVY) Military Standard Document.

3.1.1 NTDS TYPE D SERIAL OVERVIEW

The GET NTDS Type D Serial Interface Adaptors transfer 10 Mb/s binary information using bipolar serial pulse trains on two coaxial cables. An NTDS Type D I/O CHANNEL consists of a Input (Sink) Port and a Output (Source) Port, each of which can transact a 34 bit information frame using two types of 3 bit control frames. The signals required for an input transaction occur entirely on the single coaxial cable used for the Input Port. The signals required for an output transaction occur entirely on the single coaxial cable used for the Output Port.

3.2 NTDS TYPE D SERIAL TRANSACTIONS

Information transfers between two devices is accomplished using 10 Mb/s control and data frame bipolar pulse trains. The transmitting device sends a control frame requesting an eventual word transfer to the receiving equipment. The receiving equipment then sends a control frame granting or denying permission to the requesting device to transmit the data frame. If the transmission request is denied the transmitting device may elect to send another output request control frame. If the control frame indicates that permission has been granted the transmitting device sends the data frame.

3.3 NTDS TYPE D SERIAL TIMING

The encoding scheme used is called Manchester Encoding. In this scheme the transmission clock and data are encoded into each bit. This 10 Mb/s timing has a 100 nanosecond period for each bit time. Each bit time is in turn divided into two 50 nanosecond pulse periods. A logical 1 is represented by a positive pulse followed by a negative pulse. A logical 0 is a negative pulse followed by a positive pulse.

3.3.1 TYPE D INTERFACE VOLTAGES

At the transmitter end of the coaxial cable the serial data line has an amplitude of +/- 3.25 Volts. The switching threshold at the receiver end of the coaxial cable is +/- 1.25 VDC. Additionally, the receiver outputs must remain stable and not switch state for all open input conditions or when the input voltage is between 0.00 and +/- 0.5 VDC. With RG-12A coaxial cable and 75 Ohm termination the maximum specified cable length is 1000 ft (Figure 3.2).

3.3.2 CONTROL FRAME FORMAT

The first bit of each three bit control frame (Figure 3.1) pulse train is a logic 1 synchronization bit. The next two bits represent the Data and Function requests and enables. Both bits may be set in any control frame. A data or function word can be transmitted following a control frame exchange.

3.3.3 DATA FRAME FORMAT

The first bit of each thirty four bit data frame pulse train is a logic 1 synchronization bit. The next bit is the word identifier (0 for Data and 1 for Functions/Interrupts). The next 32 bits represent the transmitted data. No parity or other check bits are specified (Figure 3.2).

3.4 SERIAL INTERFACE CATEGORIES

The NTDS Type D Serial interface channels are specified to operate as Computer or Peripheral channels in order to support the three NTDS equipment categories defined in MIL-STD-1397C. These equipment categories are:

A. Category I - Computer to Peripheral
B. Category II - Computer to Computer (Inter-Computer)
C. Category III - Peripheral to Peripheral (Inter-Peripheral)

3.4.1 CATEGORY I OUTPUT OPERATION

In Category I Computer Output operation the Computer Output Channel is connected to a Peripheral Input Channel. The Computer transmits Output Enable Control Frames (OECF) with the Output Data Enable (ODE) and External Function Enable (EFE) bits indicating its readiness to transmit. The Peripheral device's Input Channel transmits Output Request Control Frames (ORCF) with the Output Data Request (ODR) and External Function Request (EFR) bits indicating its ability to receive. The actual data frame transaction follows the sequence described in Paragraph 3.5.

3.4.2 CATEGORY I INPUT OPERATION

In Category I Computer Input operation the Computer Input Channel is connected to a Peripheral Output Channel. The Peripheral transmits Input Request Control Frames (IRCF) with the Input Data Request (IDR) and External Interrupt Request (EIR) bits indicating its readiness to transmit. The Computer device's Input Channel transmits Input Enable Control Frames (IECF) with the Input Data Enable (IDE) and External Interrupt Enable (EIE) bits indicating its ability to receive (refer to Paragraph 3.5).

3.4.3 CATEGORY II OPERATION

In Category II operation the Computer Output Channel is connected to a Computer Input Channel. The transmitting Computer sends an OECF with the ODE and EFE bits indicating its readiness to transmit. The receiving Computer Input Channel interprets the OECF as an IRCF, with the ODE as the IDR and the EFE as the EIR. The receiving Computer Input Channel transmits an IECF with the IDE and EIE bits indicating its ability to receive. The transmitting Computer Output Channel interprets the IECF as an ORCF, with the IDE as the ODR and the EIE as the EFR (refer to Paragraph 3.5).

3.4.4 CATEGORY III OPERATION

In Category III operation the Peripheral Output Channel is connected to a Peripheral Input Channel. The transmitting Peripheral transmits an IRCF with the IDR and EIR bits indicating its readiness to transmit. The receiving Peripheral Input Channel interprets the IRCF as an OECF, with the IDR as the ODE and the EIR as the EFE. The receiving Peripheral Input Channel transmits an ORCF with the ODR and EFR bits indicating its ability to receive. The transmitting Peripheral Output Channel interprets the ORCF as an IECF, with the ODR as the IDE and the EFR as the EFE. The actual data frame transaction follows the sequence described in Paragraph 3.5.

3.5 SERIAL TRANSFERS

When viewed on a bit by bit basis, the data frame transaction operations between Computer and Peripheral devices is essentially the same regardless of Category. The main difference is in the control frame and bit naming conventions used. In short, the transmitter to receiver link works the same for all three categories, with the similar timing and event sequences. Therefore, only the Category 1, Computer Output to Peripheral Input transaction, will be described in detail in the following paragraphs. The transmitting device sends a control frame requesting that the receiving device accept it. The receiving device responds with a control frame indicating its ability to accept the data frame. The transmitting device, in accordance with internal priorities, sends another control frame or sends the data frame.

3.5.1 DATA FRAME TRANSFERS

Transfers of information between NTDS Input and Output devices are accomplished in two major methods: Data and Functions. An OUTPUT device sets the Output Data Enable (ODE) bit or External Function Enable (EFE) bit when it is in a condition to transmit a Data or External Function word to the INPUT device. The OUTPUT device then sends an Output Enable Control Frame (OECF) with the ODE or EFE bits (or both) set. The INPUT device responds by transmitting an Output Request Control Frame (ORCF). The ORCF indicates the INPUT Channel's ability to accept the data frame offered by the OUTPUT device, as determined by the condition of the Output Data Request (ODR) or External Function Request (EFR) bits. The active request bit indicates to the OUTPUT device that the INPUT device can accept the requested transfer. The OUTPUT device, at its convenience, sends the OD or EF data frame to the INPUT device. Note that both ODE and EFE bits may be active at any one time. The INPUT device acknowledges the receipt of data frame and its ability to accept another data frame by transmitting another ORCF frame. Figures 3.1 and 3.2 illustrate the TYPE D control and data frame formats.

3.5.2 FORCED EXTERNAL FUNCTIONS

Some NTDS computers have the ability of sending External Functions with Force and do not require that the EFR bit be set in the Input device’s ORCF. The INPUT device has no control over the rate at which External Functions with Force are sent. If the INPUT device can not accept External Functions at a high rate, timing restrictions must be made in the computer programming or external data rate buffering devices may have to be used. The typical GET TYPE D interface contains an input FIFO structure that can accept several consecutive Forced External Functions before the danger of lost data arises.

FIGURE 3.1

CONTROL FRAME TIMING

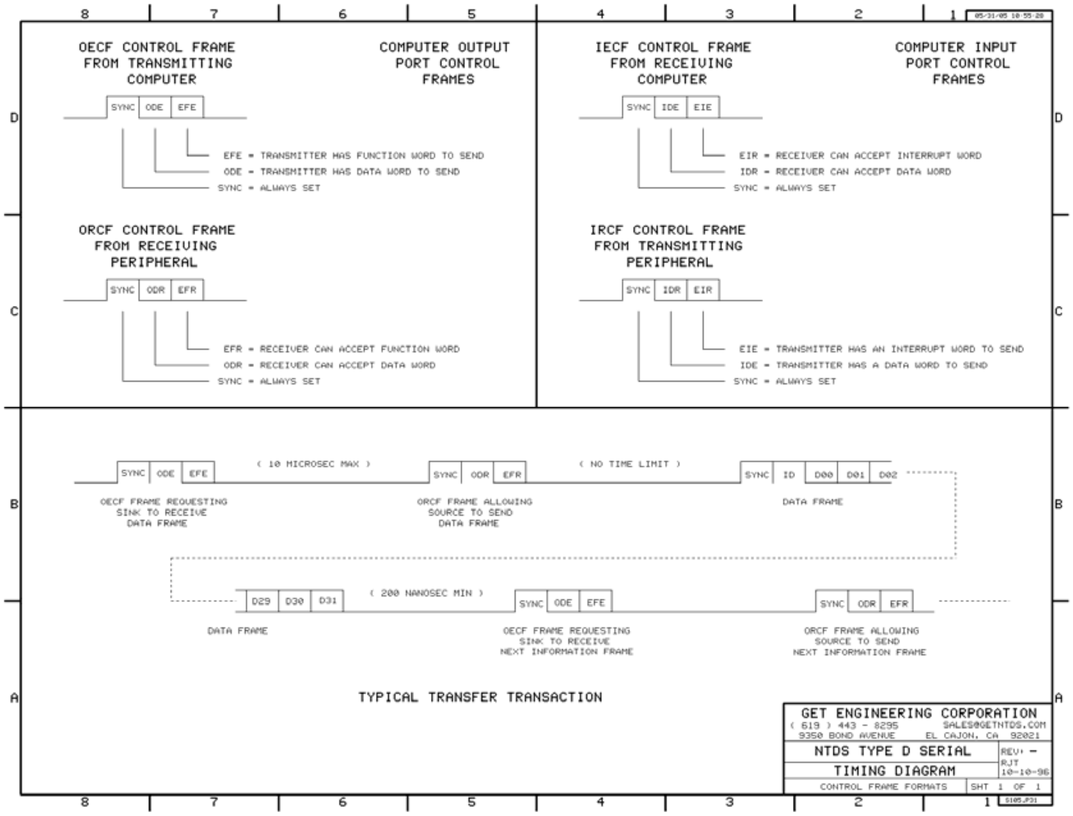
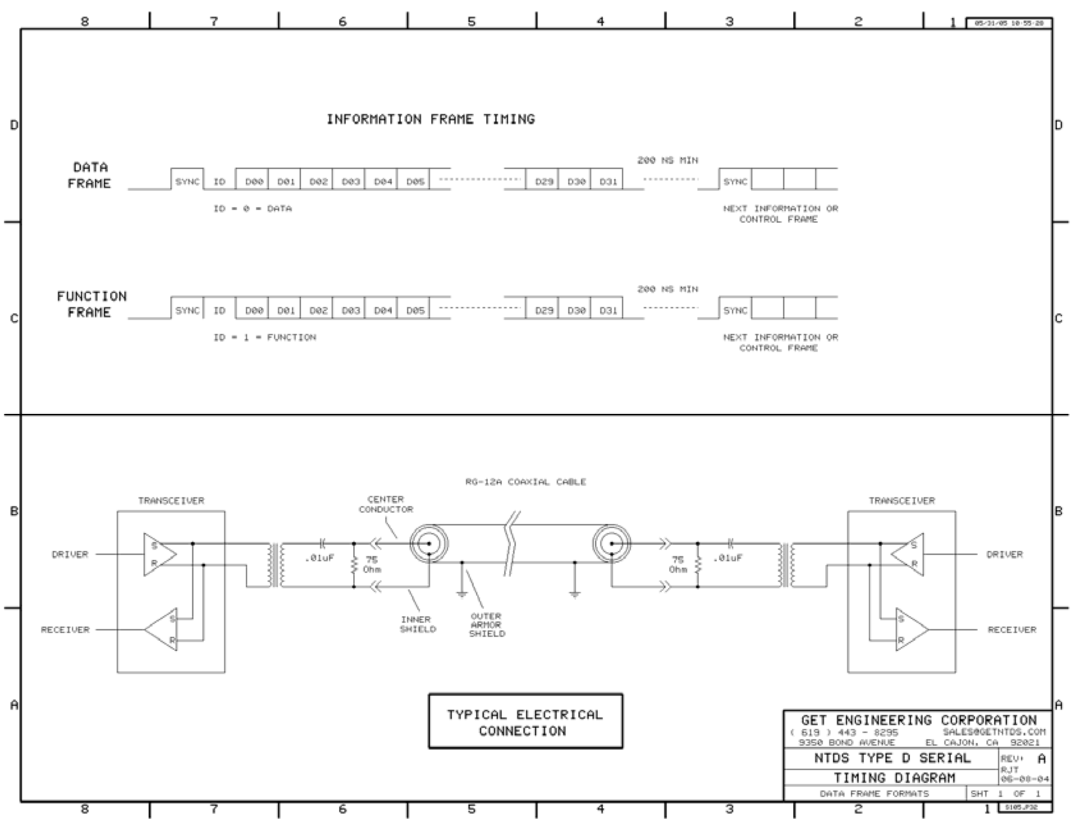


FIGURE 3.2

DATA FRAME TIMING



SECTION 4
NTDS TYPE E SERIAL INTERFACE

4.1 NTDS TYPE E SERIAL

The following discussion addresses the general design philosophy used in the design of GET NTDS Type E Serial Interface adaptors and supporting products. This discussion is intended as an aid in explaining a general operation of an NTDS Type E channel and does not cover all protocol aspects. For a complete protocol description refer to MIL-STD-1397C (NAVY) Military Standard Document.

4.1.1 NTDS TYPE E SERIAL OVERVIEW

The GET NTDS Type E Serial (LLS) Interface Adaptors transfer 10 Mb/s binary information using bipolar serial pulse trains on two triaxial cables. A LLS I/O CHANNEL consists of a Source (Output) Port and a Sink (Input) Port each of which can transact information frames using two types of 4 bit control frames. The signals required for an input transaction occur entirely on the single triaxial cable used for the Sink Port. The signals required for an output transaction occur on the single triaxial cable used for the Source Port.

4.2 NTDS TYPE E SERIAL TRANSACTIONS

Transfers of information between two serial devices is accomplished using 10 Mb/s control and data frame bipolar pulse trains. The transmitting device sends a control frame requesting an eventual word transfer to the receiving equipment. The receiving equipment then sends a control frame granting or denying permission to the requesting device to transmit the data frame. If the transmission request is denied the transmitting device may elect to send another output request control frame. If the control frame indicates that permission has been granted the transmitting device sends the data frame.

4.3 NTDS TYPE E SERIAL TIMING

The encoding scheme used is called Manchester II Split Phase Encoding. In this scheme the transmission clock and data are encoded into each bit. This 10 Mb/s timing has a 100 nanosecond period for each bit time. Each bit time is in turn divided into two 50 nanosecond pulse periods. A logical 1 is represented by a positive pulse followed by a negative pulse. A logical 0 is a negative pulse followed by a positive pulse.

4.3.1 TYPE E INTERFACE VOLTAGES

At the transmitter end of the coaxial cable the serial data line has an amplitude of +/- .600 Volts. The switching threshold at the receiver end of the coaxial cable is +/- .220 VDC. Additionally, the receiver outputs must remain stable and not switch state for all open input conditions or when the input voltage is between 0.00 and +/- 0.155 VDC. The receiver input circuits must also be able to reject input transient pulses of specific energy levels. With MIL-C-17/134 triaxial cable and 50 Ohm termination the maximum specified cable length is 390 ft. With MIL-C-17/135 triaxial cable and 50 Ohm termination the maximum specified cable length is 980 ft (Figure 4.1).

4.3.2 CONTROL FRAME FORMAT

There are two types of control frames used in the LLS transaction protocol (Figure 4.2). The Source Status Control Frame (SOS) is used by the Source device to indicate its readiness to transmit Information Frames. The Sink device uses the Sink Status Control Frames (SIS) to indicate its readiness to receive. The first bit of these four bit control frames is a logic 1 synchronization bit. The next two bits represent the Data and Function requests and enables. Both bits may be set in any control frame. The fourth control frame bit is the control frame identifier bit (ID). The polarity of the ID bit is user selectable on GET interface adaptors.

4.3.3 INFORMATION FRAME FORMATS

The information frame transmitted as a result of the control frame exchange is identified by the information word identifier bit (Figure 4.3). There are two types of Information Frames (IF) used. The Single Word Transfer (SWT) Frames transfer single 34 or 35 bit Data or Command/Interrupt (CIW) words. The Burst transfer frame is used to send up to 32 Data words in a single transaction. The first bit of each IF is a logic 1 synchronization bit. The next bit is the word identifier (WI, 0 for Data and 1 for CIW). The next 32 bits represent the transmitted data, followed by an optional ODD parity bit. For burst frames, up to 31 additional Data words, with optional parity, follow. CIWs can not be sent as Burst frames.

4.4 SERIAL TRANSFERS

A SOURCE device sets its Output Data Enable (ODA) line or External Function Enable (EFA) line when it is in a condition to transmit a Data or CIW word to the SINK device. The SOURCE device then sends a SOS frame with the ODA or EFA bits set. The SINK device responds to the SOS by transmitting a SIS frame. The SIS indicates the SINK port's ability to accept the data frame offered by the SOURCE device with the Output Data Request (ODR) and External Function Request (EFR) bits. The active request bit indicates to the source device that the SINK device can accept the requested transfer. Note that both ODR and EFR bits may be active at any one time. The SOURCE device, at its convenience and according to internal priorities, sends the SWT or Burst IF to the SINK device. The SINK device acknowledges the receipt of data and its possible ability to accept another IF by sending another SIS frame.

4.4.1 FORCED EXTERNAL FUNCTIONS

Some NTDS devices have the ability of sending a Forced CIW and do not require that the EFR bit be set in the SIS frame. The SINK device has no control over the rate at which CIWs with Force are sent. If the SINK device can not accept the CIWs at a high rate, timing restrictions must be made in the computer programming or external data rate buffered devices may have to be used. The GET interface adaptors contain input FIFO buffers that can accept several consecutive Forced CIWs before the danger of lost data arises.

4.5 SYSTEM INTEGRITY FEATURES

The LLS System Integrity Features (SIF) are designed to improve system reliability. Using SIF, the user can determine if an LLS interface is improperly connected, disabled, or malfunctioning. The SIF error detection logic is designed to detect communications loss, protocol violations, and data corruption. The SIF monitors are designed to operate simultaneously and without interfering with normal LLS protocol operations. The monitored error conditions include Sink and Source port CF timeouts, IF parity, CF validation, CF and IF framing errors, and CF and IF response errors. No corrective action is specified if a SIF error is detected. However, when a SIF error condition is detected the operator must be notified by appropriate register settings or, if implemented, a status indicator.

FIGURE 4.1

LLS ELECTRICAL CONNECTIONS

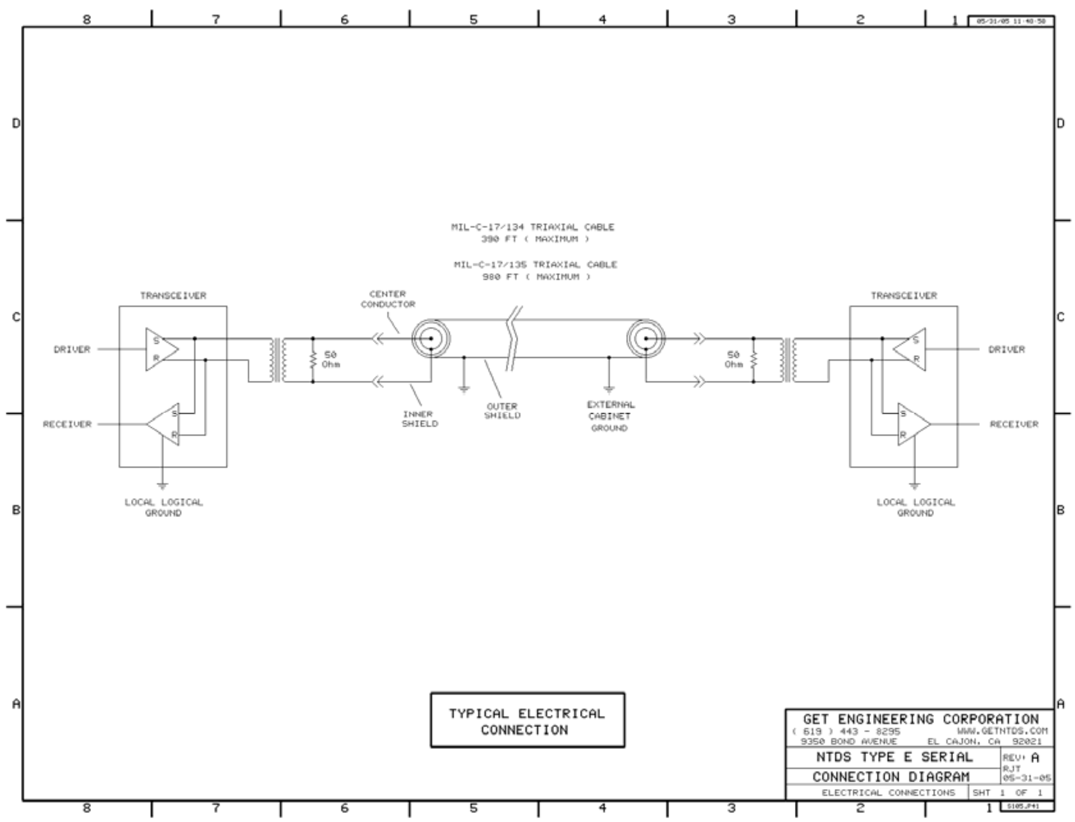


FIGURE 4.2

LLS CONTROL FRAME TIMING

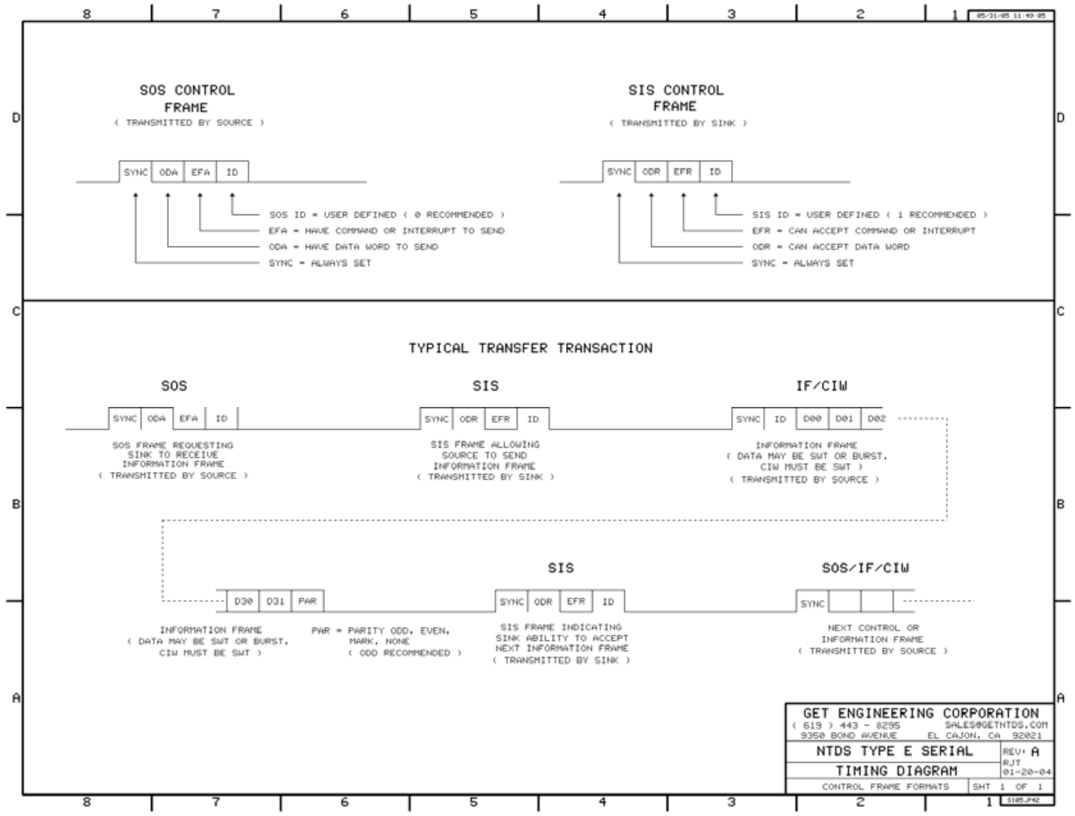
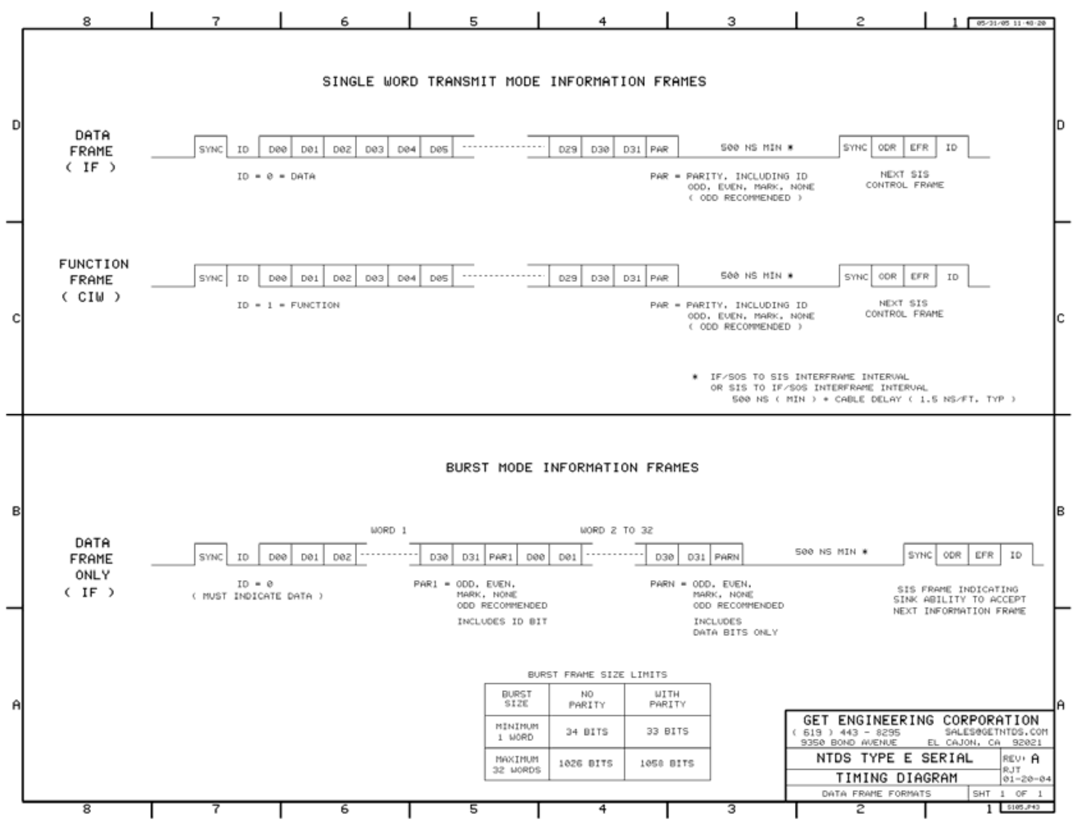


FIGURE 4.3

LLS DATA FRAME TIMING



SECTION 5
GET NTDS INTERFACE ADAPTORS
KEY OPERATIONAL FEATURES

5.1 GENERAL ORGANIZATION

The GET NTDS interface adaptors are divided into three major functional modules including the NTDS Input Port, NTDS Output Port, and the local host Bus Interface and controller (Figure 5.1). The structure and operation of the NTDS ports is identical for all interface types and the functional descriptions provided apply to all GET NTDS interface adaptors.

5.2 NTDS INPUT PORT

The NTDS Input Port (serial SINK) accepts data from the attached device and consists of the Input Register, the Input FIFO, and the Extract Register. Transaction timers monitor the operation of the Input and Extract ports and alert the system software when a command or transaction timeout condition exists. From the perspective of the externally connected NTDS device the Input and Extract Registers form a single NTDS Input Port. The Input Register data path is intended for use for large volume transactions and is connected to a DMA controller. The Input FIFO provides the ability to transact and buffer the NTDS data without compromising the system bus bandwidth. The Extract Register is intended for single word transactions and is serviced directly by the system processor. The Input and Extract Registers operate independently and both may be active at any one time.

5.2.1 INPUT PORT DATA PATH

Received NTDS data is transferred from the Input Port to system memory using the Input Register DMA or Extract Port facilities. The Input Data initially passes through the Input Data Receivers to the Input FIFO or to the Extract Register. The Input FIFO architecture provides automatic sorting of Input Data and other requested transactions (Terminating transactions and Forced Functions) while maintaining timing coherency. The Input FIFO also serves as a caching rate buffer which allows NTDS Input Data to be received at the highest allowable rate, regardless of system bus capacity. The DMA controller and FIFO also serve as a rate buffer that allows the NTDS data to be assembled and transferred to memory at the maximum allowable system bus rate. The Extract path data consists of a single 32 bit register which is directly accessed by the system processor.

5.3 NTDS OUTPUT PORT

The NTDS Output Port (serial SOURCE) sends data to the attached device and consists of the Output Register and the Insert Register. From the perspective of the externally connected NTDS device the Output and Insert Registers form a single NTDS Output Port. The Output Register is intended for use for large volume transactions and is connected to the DMA controller. The DMA FIFO provides the ability to assemble and buffer the NTDS data without compromising the system bus bandwidth. The Insert Register supports single word transactions and must be directly serviced by the system processor. The Output and Insert Registers operate independently and may be simultaneously active.

5.3.1 OUTPUT PORT DATA PATH

Data is transferred from system memory to the Output Port using DMA or Insert Port facilities. The DMA transfers pass through the system bus interface to the Output Register and then to the Output Data Drivers, which hold the actual NTDS data being transacted. The Insert path data consists of a single 32 bit Insert Data Register which is directly accessed by the system processor.

5.4 PROTOCOL OPERATIONS

Modern communication protocols generally consist of a set of Request and Acknowledge transactions to negotiate the transfer of blocks of data. A typical example of this process is illustrated in Figure 5.3 (A & B). All GET interface adaptors support Half Duplex and Full Duplex protocol operations. Full duplex protocol operations are possible because all Input Port and Output Port components are independent and may be active at any time.

5.4.1 HALF DUPLEX OPERATIONS

Half Duplex channels are generally found on peripheral devices like tape drives, display systems, and printers. In these systems all operations are CPU initiated and data buffers are transferred in only one direction at a time. In other words either the input buffer or the output buffer may be active at one time. The protocol normally consists of an EF command code word followed by the required OD or ID. At the end of the command the peripheral device may issue a status EI code word (Figure 5.2). Data and command coherency (the order in which OD/ID and EF/EI are transferred) are very important in these systems as the EF/EI transfers are generally used to bound the OD/ID buffers.

5.4.1.1 HALF DUPLEX SUPPORT

Half Duplex protocol operations with built in data and command coherency are easily performed using the Output and Input Ports. Output Commands (Figure 5.2A) can be transmitted using the Split Buffer Output feature. This operation will transmit an EF followed by the OD buffer. Command completion can be specified to be the end of buffer, interword timeout, or Buffer/Command timeout. The received EI status word can then be read out using the Read Function command. Input Commands (Figure 5.2B) are transmitted using the Output Function feature and the required ID can be received using the Receive Data with Abort on Function feature. This operation will transmit an EF followed by the opening of an ID buffer. Command completion can be specified to be the end of buffer, reception of the EI status word, interword timeout, or Buffer/Command timeout. The received EI word can be read out using the Read Function command.

5.4.2 FULL DUPLEX OPERATIONS

Full Duplex operations are generally used on inter-computer channels and intelligent peripheral devices like navigation systems and data processors. In these systems either device may independently initiate a data transfer and the input and output buffers may both be active simultaneously. The protocol normally consists of an EF and EI exchange to negotiate the buffer transfer followed by the required OD or ID buffer. The transmitting device may optionally send an end of command EI status word. Data and command coherency are less important in these systems as the EF/EI code words are used to enable the data buffers rather than to bound them (Figure 5.3).

5.4.2.1 FULL DUPLEX SUPPORT

Full Duplex protocol operations are performed on GET interface adaptors using the single word Insert and Extract ports for the EF/EI operations and the Output and Input Ports for the OD/ID buffers. Command completion can be specified to be the end of buffer, interword timeout, or Buffer/Command timeout.

5.5 INTERVAL TIMERS

The Input and Output ports each contain a set of interval timers that are used as a Command or Buffer timer and an interword timer (Figure 5.4). The Insert and Extract registers only have Command timers. These timers have 1 microsecond clocking granularity and automatic stop/start controls. These timers are automatically disabled at buffer completion.

5.5.1 TRANSACTION QUALITY TIMING

Most tactical devices have specified command response times and data transfer rates that must be met in order to be considered fully operational. As an interface quality control mechanism, timeouts can be used to indirectly indicate the operational status of these devices. Limit values for the Buffer and Interword timers can be calculated using the specified response times, transfer rates, and buffer size information.

5.5.2 COMMAND/BUFFER TIMEOUT TIMER

The Command/Buffer Timeout Timer generates an interrupt signal when the timer expires. The timer is initialized by loading a value representing the desired timeout period. Values from 1 microsecond to 36 minutes can be used. When the Command Timeout Mode is selected the timer countdown starts when the command is started. When the Buffer Timeout Mode is selected and the timer countdown starts on the initial SET to CLEAR transition of the data ready status bit (indicating that the first word of the buffer has been transacted).

5.5.3 INTERWORD TIMEOUT TIMER

The Interword Timeout Timer generates an interrupt when the specified time between NTDS transactions is exceeded. Timeout values from 1 microsecond to 65 seconds can be used. The timer countdown starts on the initial SET to CLEAR transition of the data ready status bit (indicating that the first word of the buffer has been transacted). The timer is automatically reinitialized each time the data ready status is set.

5.5.3.1 END OF BUFFER TIMEOUT

The Interword Timeout Timer can be used to determine actual buffer size in systems (such as tape drives) which have variable or undetermined buffer sizes. An Input or Output command with a buffer size larger than the maximum expected can be started. If a timeout value larger than the maximum expected time between data transfers is specified, an Interword Timeout interrupt will be generated when the device stops transacting data (the end of it’s buffer). This timeout can be interpreted as the end of buffer signal.

FIGURE 5.1

INTERFACE CONFIGURATION

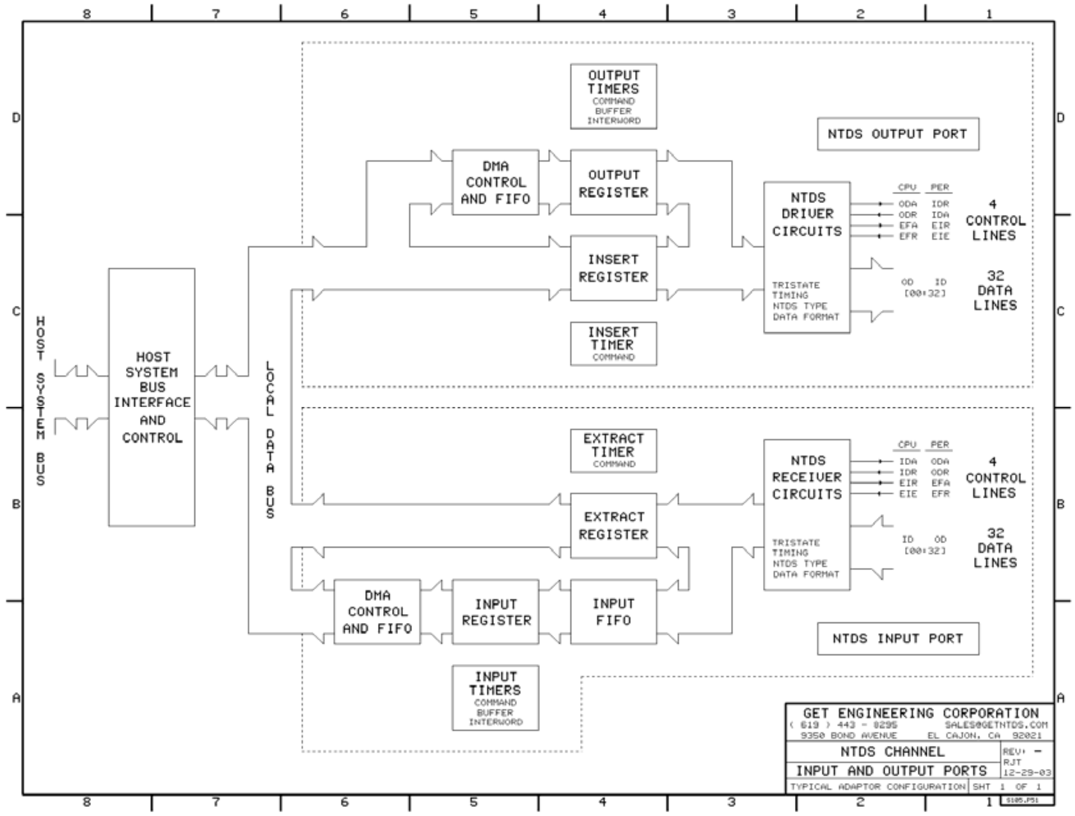


FIGURE 5.2

HALF DUPLEX OPERATION

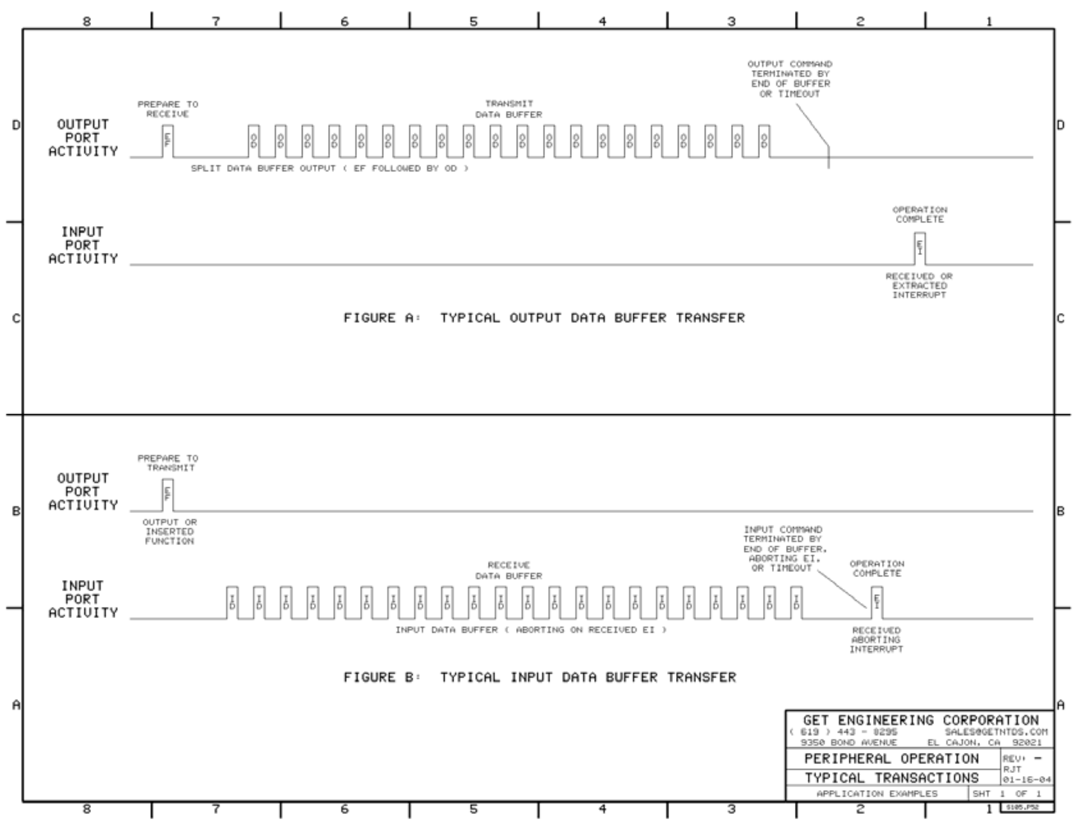


FIGURE 5.3

FULL DUPLEX OPERATION

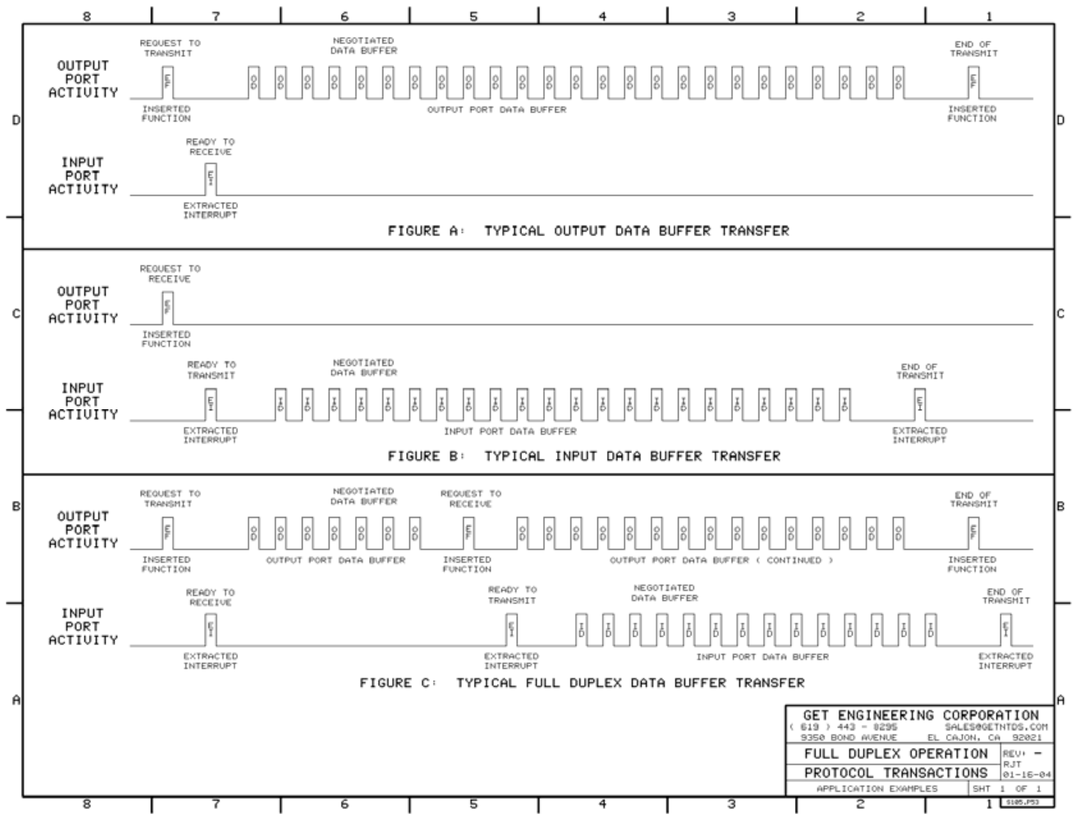
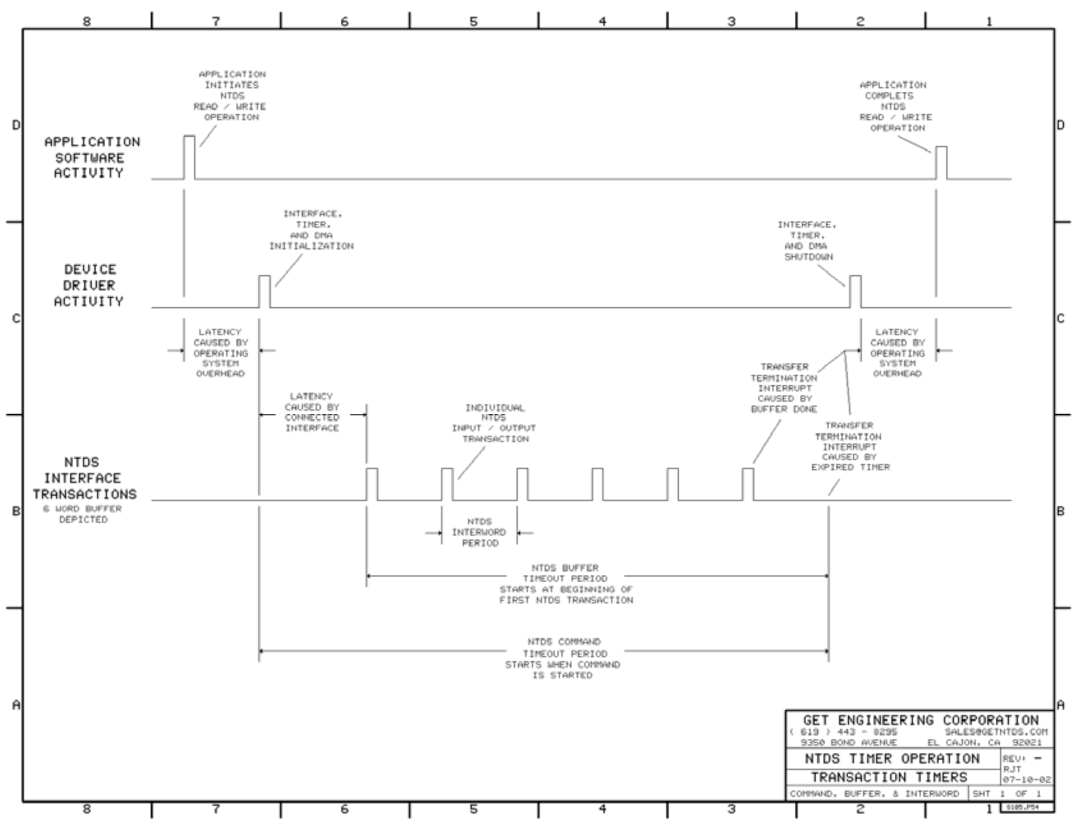


FIGURE 5.4

TRANSACTION TIMEOUT OPERATION



SECTION 6
ATDS SERIAL INTERFACE

6.1 ATDS SERIAL OVERVIEW

The following discussion is a brief operational description of a typical ATDS serial channel. It is intended as an aid in explaining the operation of this link and as such does not cover all aspects of the ATDS communication protocol. Refer to MIL-STD-188-203-1A (Appendix D2) Military Standard Document for a complete description of ATDS data exchange protocols.

6.2 SERIAL TRANSFERS

Transfers of information between ATDS Data Terminal Sets (DTS) and Tactical Data System (TDS) Computers are accomplished on a single cable in a complex half duplex mode (Figure 6.4). Three transfer operations are used: DTS to TDS data, TDS to DTS data, and TDS to DTS Address transfers.

6.2.1 DTS TO TDS DATA TRANSFERS

Data transfers from the DTS to the TDS computer are performed using the Frame, Data Clock, Incoming Data, and Outgoing Data Lines (Figure 6.1). The DTS generates a pulse on the Frame line when it desires to transmit a data frame to the TDS computer. When the computer is ready to receive, it issues a series of 26 pulses on the Data Clock Line to shift the serial data on the Incoming Data Line from the DTS to the computer. After a minimum delay of 7 microseconds the computer generates a second series of 26 clock pulses which resends the same serial data from the DTS to the computer again. The computer then compares the two received data words and, if they are not identical, generates a fault pulse on the Outgoing Data Line.

6.2.2 TDS TO DTS DATA TRANSFERS

Data transfers from the TDS computer to the DTS are performed using the Frame, Data Clock, Incoming Data, and Outgoing Data Lines (Figure 6.2). The DTS generates a pulse on the Frame line when it desires to receive a data frame from the TDS computer. When the computer is ready to transmit, it issues a series of 26 pulses on the Data Clock Line to shift the serial data on the Outgoing Data Line from the computer to the DTS. After a minimum delay of 7 microseconds the computer generates a second series of 26 clock pulses which returns the serial data just received from the computer back to the computer. The computer then compares the two received data words and, if they are not identical, generates a fault pulse on the Outgoing Data Line.

6.2.3 TDS TO DTS ADDRESS TRANSFERS

Address Frame transfers from the Tactical Data System computer to the DTS are performed using the Frame, Incoming Data, and Address Data, and Address Clock Lines (Figure 6.3). When the DTS desires to receive an address frame from the TDS computer it generates a simultaneous pulse on the Frame and Incoming Data lines. When the computer is ready to transmit, it issues a series of 7 pulses on the Address Clock Line to shift the serial data on the Address Data Line from the computer to the DTS.

6.2.4 DTS TO TDS DATA FORMAT

The 26 bit DTS to TDS serial data frame consists of two leading Control Bits (C1 and C2) followed by 24 Data Bits. The Control bits are used to indicate the quality of the received data. Control Bit C1 is generally used to indicate the presence of detected errors in the data field. Control Bit C2 is used as the frame start indication. This bit is SET in the first frame and CLEAR for all subsequent frames of each message.

6.2.5 DTS TO TDS ADDRESS FORMAT

The 7 bit DTS to TDS serial address frame consists of 6 leading Address Bits followed by a single Message Control Bit. The Message Control bit is typically used to define the message format to be used by the DTS during transmission.

6.2.6 TDS TO DTS DATA FORMAT

The 26 bit TDS to DTS serial data frame consists of two leading Control Bits (C1 and C2) followed by 24 Data Bits. The Control bits are used to indicate the type of the transmitted data. The data frame is valid when Control Bits C1 and C2 are both SET. A stop condition is indicated when either C1 or C2 are CLEAR. In this case the DTS will typically discard the data portion of the frame and transmit a special stop code.

6.3 SIDETONE INTERFACE OPERATION

The Sidetone Frame, Sidetone Data, and Sidetone Clock lines are used for test and data validation purposes. The Sidetone Interface provides an additional echo data path that returns to the TDS computer the data that was transmitted by the DTS.

6.3.1 DTS TO TDS SIDETONE TRANSFER

The 26 bit TDS to DTS serial data frame consists of two leading Control Bits followed by 24 Data Bits. The Sidetone transfers from the DTS to the TDS computer are performed using the Sidetone Frame, Sidetone Data, and Sidetone Data Clock (Figure 6.3). The DTS generates a pulse on the Sidetone Frame line when it desires to transmit a Sidetone Data frame to the TDS computer. When the computer is ready to receive, it issues a series of 26 pulses on the Sidetone Clock Line to shift the serial data on the Sidetone Data Line from the DTS to the computer. The computer then uses the received Sidetone Data to evaluate the transmission performance of the DTS.

6.4 ELECTRICAL CHARACTERISTICS

The signal interface lines between the TDS computer and the DTS are measured across a 100 Ohm load on the secondary winding of a terminating transformer. The amplitude of all pulses is -6 VDC, with respect to ground. This voltage is 0.0 VDC when no pulses are present. The width of the pulses from the TDS to the DTS is 200 nanosec. The width of the pulses from the DTS to the TDS is 600 nanosec. The nontatical interface (sidetone) lines have open collector drivers with the capability of sinking 20 mA to ground. The amplitude of the sidetone signals is nominally +5 VDC, with respect to ground. The sidetone receiver switching threshold is 1.5 VDC.

FIGURE 6.1

DTS TO TDS DATA FRAME TIMING

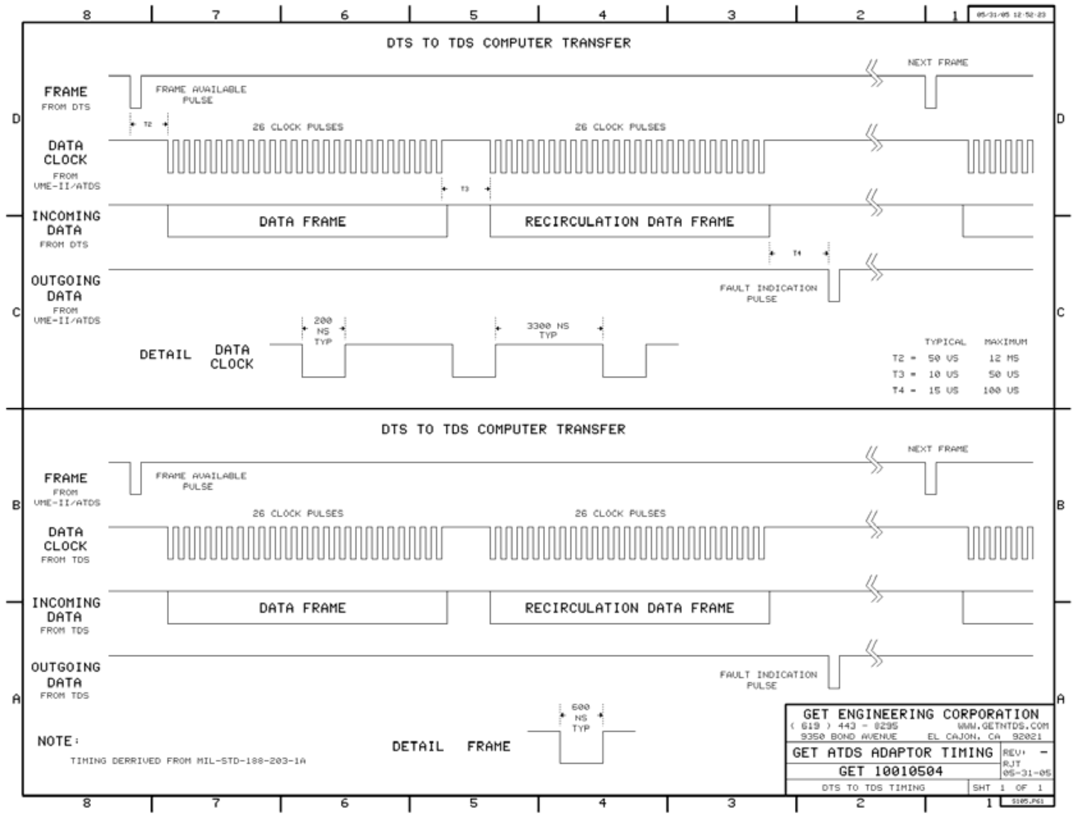


FIGURE 6.2

TDS TO DTS DATA FRAME TIMING

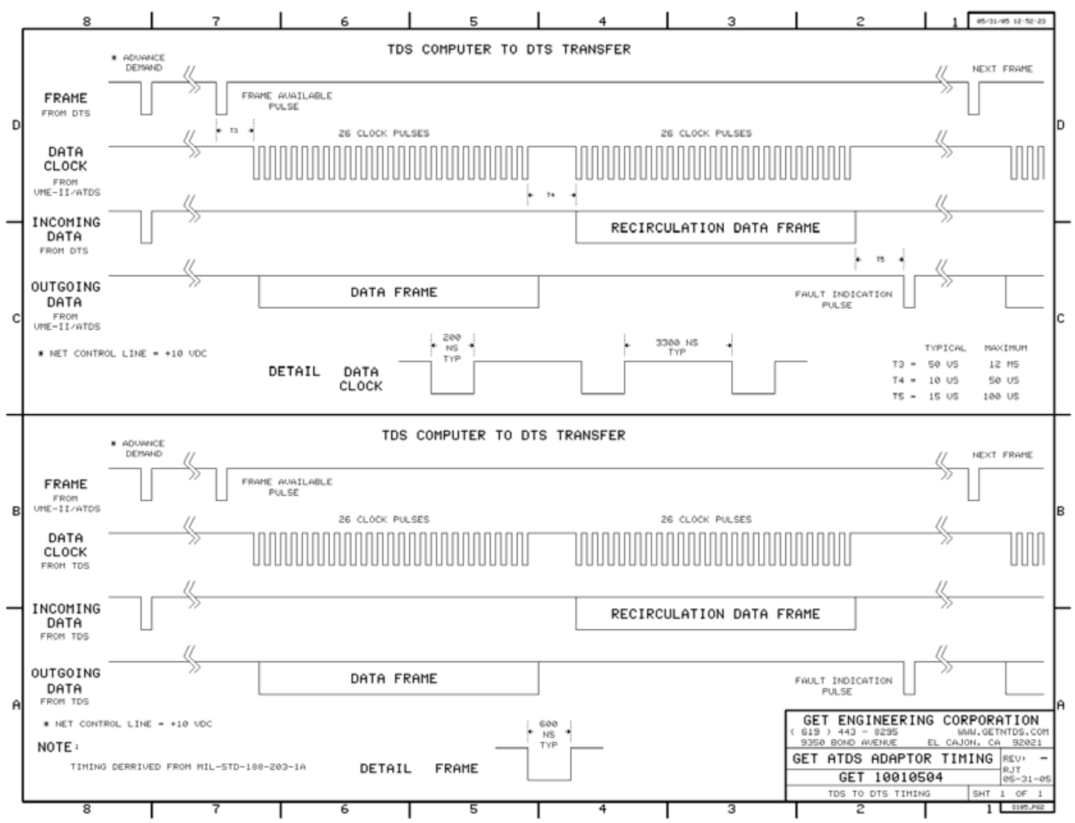


FIGURE 6.3

SIDETONE AND ADDRESS FRAME TIMING

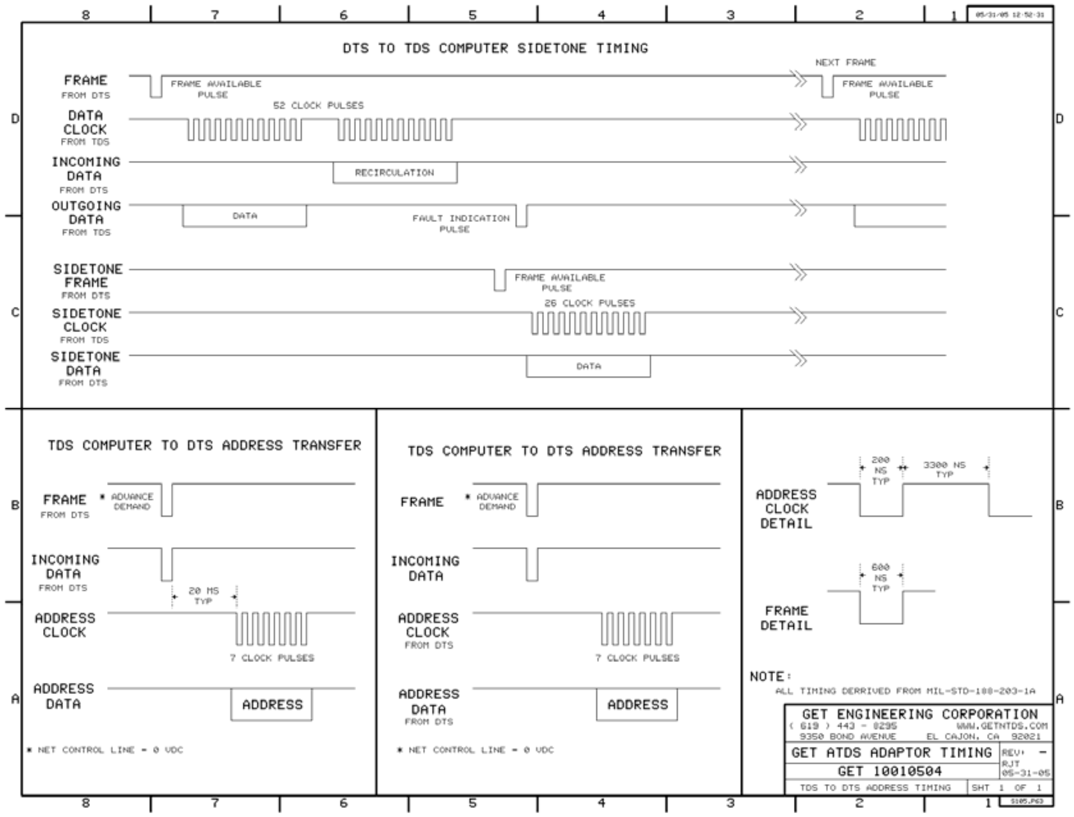
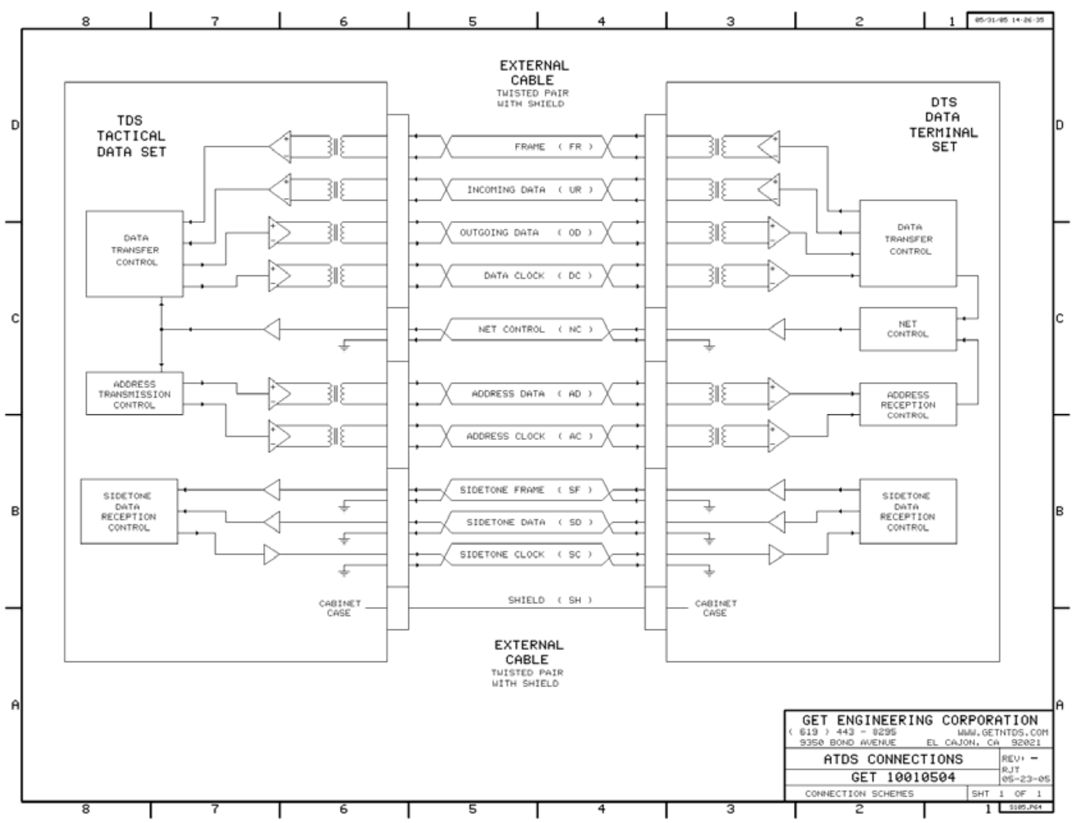


FIGURE 6.4

ATDS ELECTRICAL CONNECTIONS



SECTION 7
PASSIVE TAP MONITOR

7.1 GENERAL PRODUCT DESCRIPTION

All GET Engineering NTDS interface adaptors can be configured to operate as passive channel activity monitors (TAP). One or more NTDS Parallel or Serial interface adaptors, in any mix, can be combined to form a complete multichannel monitoring system (Figures 7.1 and 7.2). The passive interface acts as an invisible channel activity observer and does not participate or interact with the connected NTDS port in any way. A comprehensive channel transaction analyzer is created when coupled with available software drivers and application programs (Figure 7.4). The ability to record and display real-time channel activity enables the user to easily isolate and troubleshoot complex communications failures.

7.1.1 GENERAL OPERATIONAL DESCRIPTION

The interface monitors the activity of the NTDS control signals and, when a valid transaction is detected, the corresponding data word, transaction type, and time tag are recorded (Figures 7.5 and 7.6). The TAP monitor begins transaction recording and event data collection based on specific triggering conditions. When this trigger condition is detected the user specified NTDS transactions and other events are collected in real-time and stored in a Data Collection FIFO for transfer to system memory. The recording process continues until it is suspended by the detection of a user specified check or termination condition. The recorded data can be processed in real-time or off line.

7.1.2 NTDS PARALLEL CHANNELS

The GET Parallel Channel NTDS Interface Adaptors have one Receive Port which can always operate as a passive TAP. The standard Transmit Port can not be used for TAP operations. However, most adaptors feature a TAP mezzanine module which allows the Transmit port to operate as a passive TAP. The 32 bit TAP ports can be software configured to operate in NTDS SLOW, FAST, ANEW, or Type H environments and can monitor transactions on Category I, II, or III connections. The typical NTDS TAP block diagram is illustrated in Figure 7.3.

7.1.3 NTDS SERIAL CHANNELS

Two types of NTDS Serial Channel Interface Adaptors allow TAP operation in Type D and Type E environments. These adaptors have two ports which can operate as passive TAPs. These 32 bit NTDS ports can be software configured to operate with all Parity, Control Frame, and SIF options.

7.2 GENERAL OPERATING DESCRIPTION

The TAP operation is identical regardless of system bus (PCI, PMC, PC/104+, cPCI, or VME) or adaptor type (Parallel or Serial). The recording process is divided into five functional steps and closely resembles the operation of a typical logic analyzer (Figure 7.5). These steps include pretrigger transaction recording, trigger word detection and recording, specified transaction recording, check word detection and recording, and post-check transaction recording.

7.2.1 GENERAL TAP OPERATION

The TAP is initially configured to match the interface to which it is connected. These configuration options are software selectable (Table 7.1). Recording trigger, filter, check, and termination parameters are then loaded into the TAP command fields and the TAP is started. Transaction recording starts when the prescribed trigger condition is encountered. A time tag synchronization signal is generated notifying other TAP channels that a trigger condition has been detected. Each transaction is analyzed according to the filtering criteria, and if it is qualified, it is recorded. This recording process continues until a specified check condition is detected. At that time the TAP can be stopped or automatically restarted, based on a set of predefined parameters. A termination signal is generated notifying other TAP channels that a termination condition has been detected. A typical TAP recording session is depicted in Figure 7.6.

7.2.2 TAP DATA FORMATS

Specified NTDS transactions or events are collected, formatted, and loaded into a Data Collection FIFO for transfer to system memory. The TAP recording buffer will contain a detected trigger or sync word, any number of recorded transaction and TAP event words, a possible check word, a possible number of post-check transaction words, and a termination event word. All NTDS transactions are recorded as 32 bit elements. The recorded transaction and event word formatting consists of a 32 bit data field with an appended 24 bit timestamp (100 ns or 125 ns resolution) and an 8 bit status byte. The adaptor dependent status byte describes the transaction recording conditions.

7.3 TAP SOFTWARE DESCRIPTION

The GET NTDS Channel Analyzer System software program, GET 55701741, is available for controlling TAP configured interface adaptors. This full featured Windows (WDM, NT) application program provides all of the functions and utilities which allow the user to fully configure and control the TAP interface. Single and multiple interface adaptor systems are supported. When used with the available Windows NT PCI TAP Driver (GET 50701741), the low order control, configuration, synchronization, and data display functions are handled by the program. Figure 7.4 shows some typical TAP Software screens.

7.4 NTDS PARALLEL CHANNEL OPERATION

An NTDS Parallel channel consists of an Input and an Output Port, each of which contain up to 32 data lines and four control lines. The transfer of data over the NTDS ports is controlled by the operation of these control lines. The operation of these NTDS channels is described in other sections of this document. For a complete description of NTDS data exchange protocols refer to MIL-STD-1397C (SHIPS) Military Standard Document.

7.4.1 PARALLEL CHANNEL TAP OPERATION

The TAP Port records transactions and events based on the activity of the four NTDS control lines. When connected to an NTDS Output Port the transaction information is collected on the low to high transition of the ODA or EFA lines. The EFR line is used to indicate if the transaction was performed with force. When connected to an NTDS Input Port the transaction information is collected on the low to high transition of the IDA line. The IDR, EIR, and EIE lines are used to indicate the type of transfer performed (Figure 7.7).

FIGURE 7.1

NTDS PARALLEL INTERFACE ADAPTOR - TAP CONNECTIONS

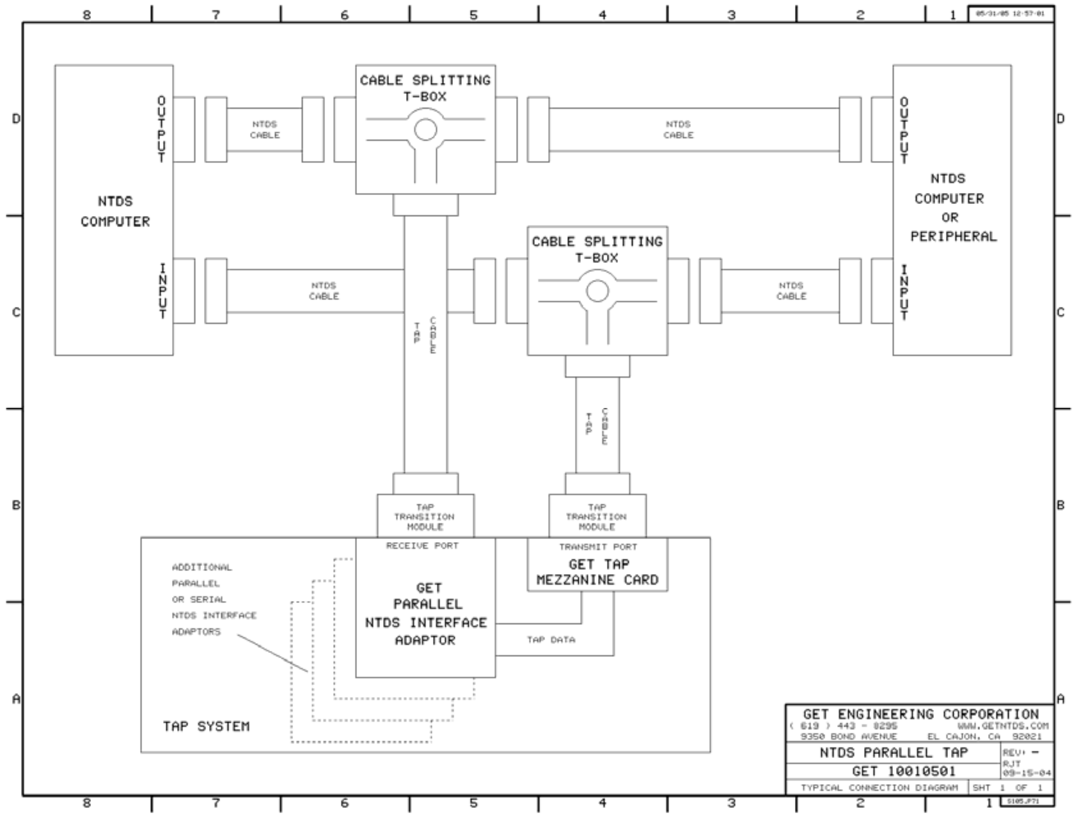


FIGURE 7.2

NTDS SERIAL INTERFACE ADAPTOR - TAP CONNECTIONS

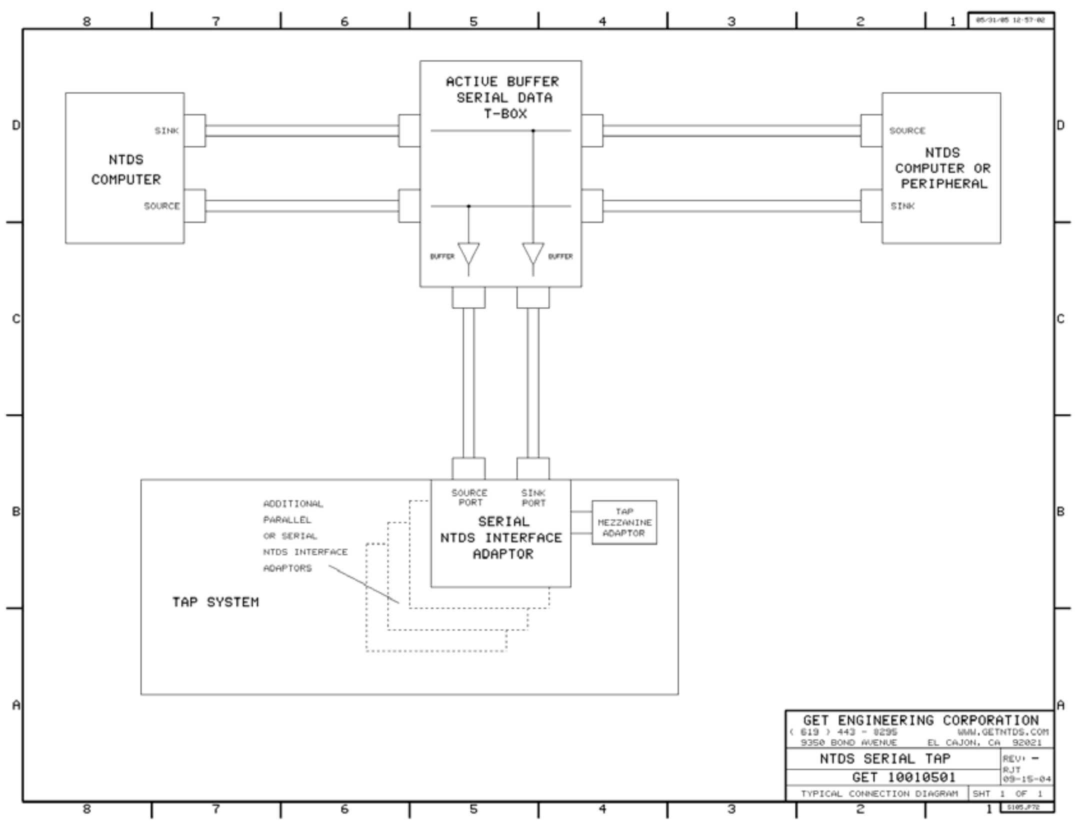


FIGURE 7.3

NTDS INTERFACE ADAPTOR – TAP FUNCTIONAL BLOCK DIAGRAM

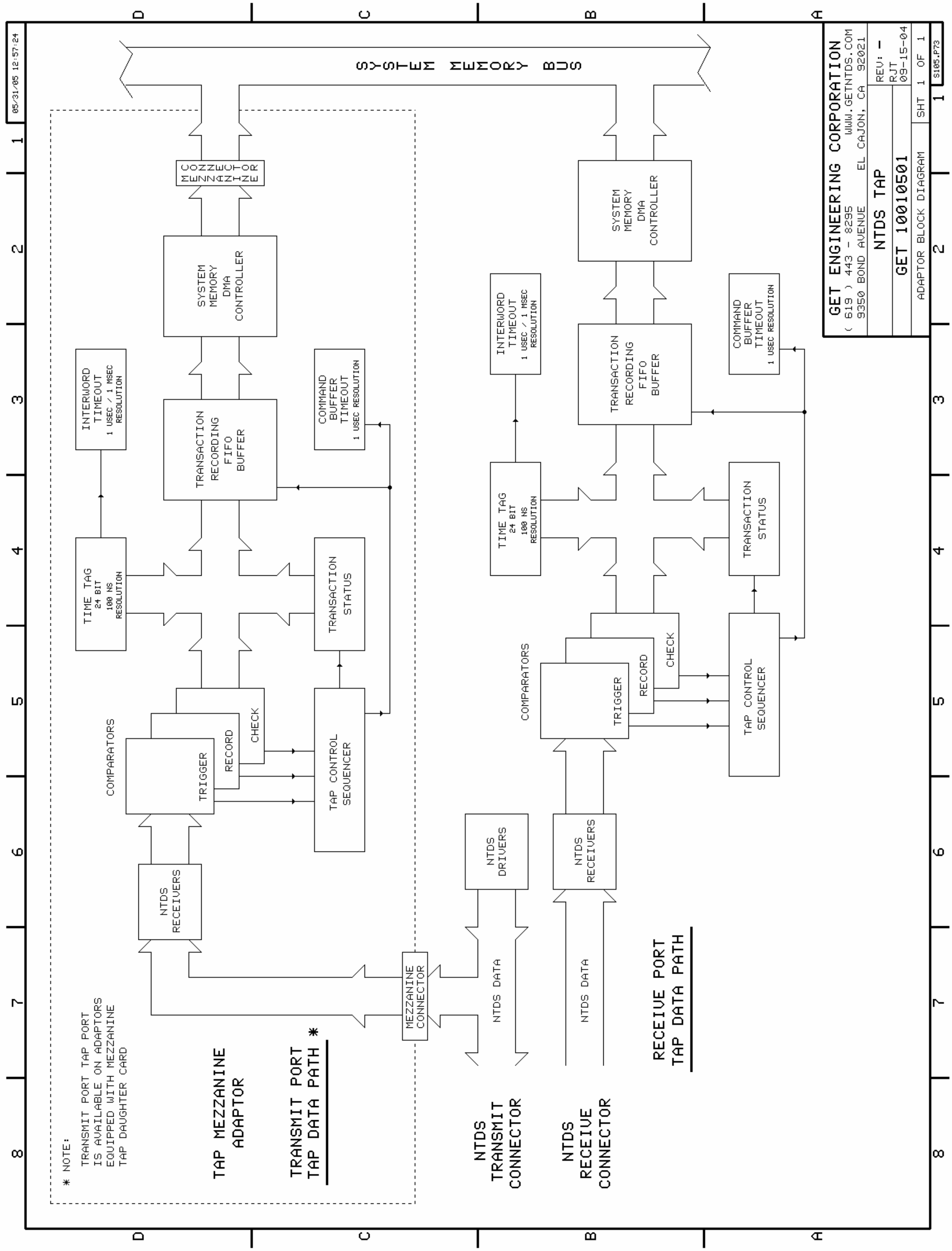


FIGURE 7.4

NTDS TAP SOFTWARE SCREEN

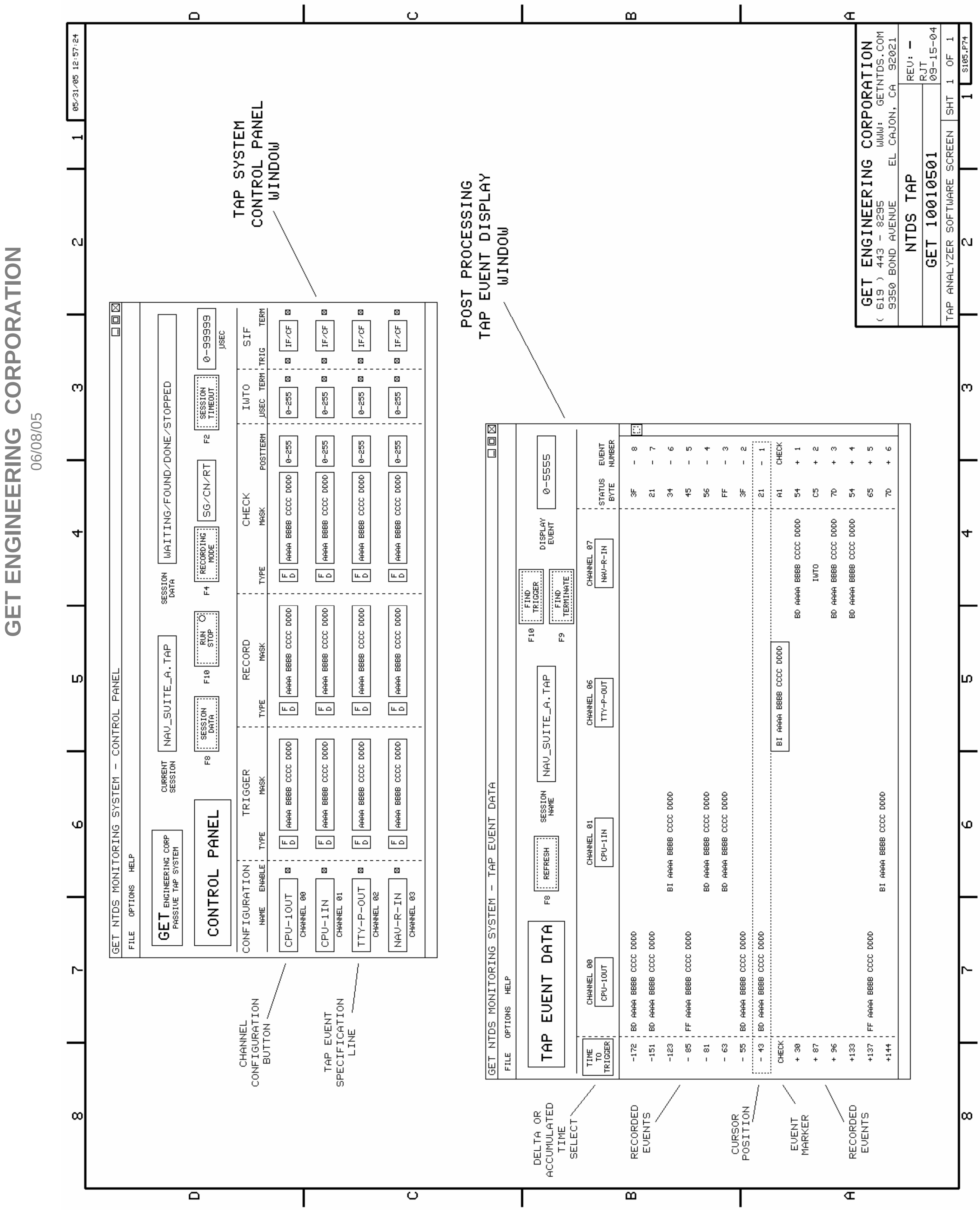


FIGURE 7.5

NTDS TAP FUNCTIONAL FLOW

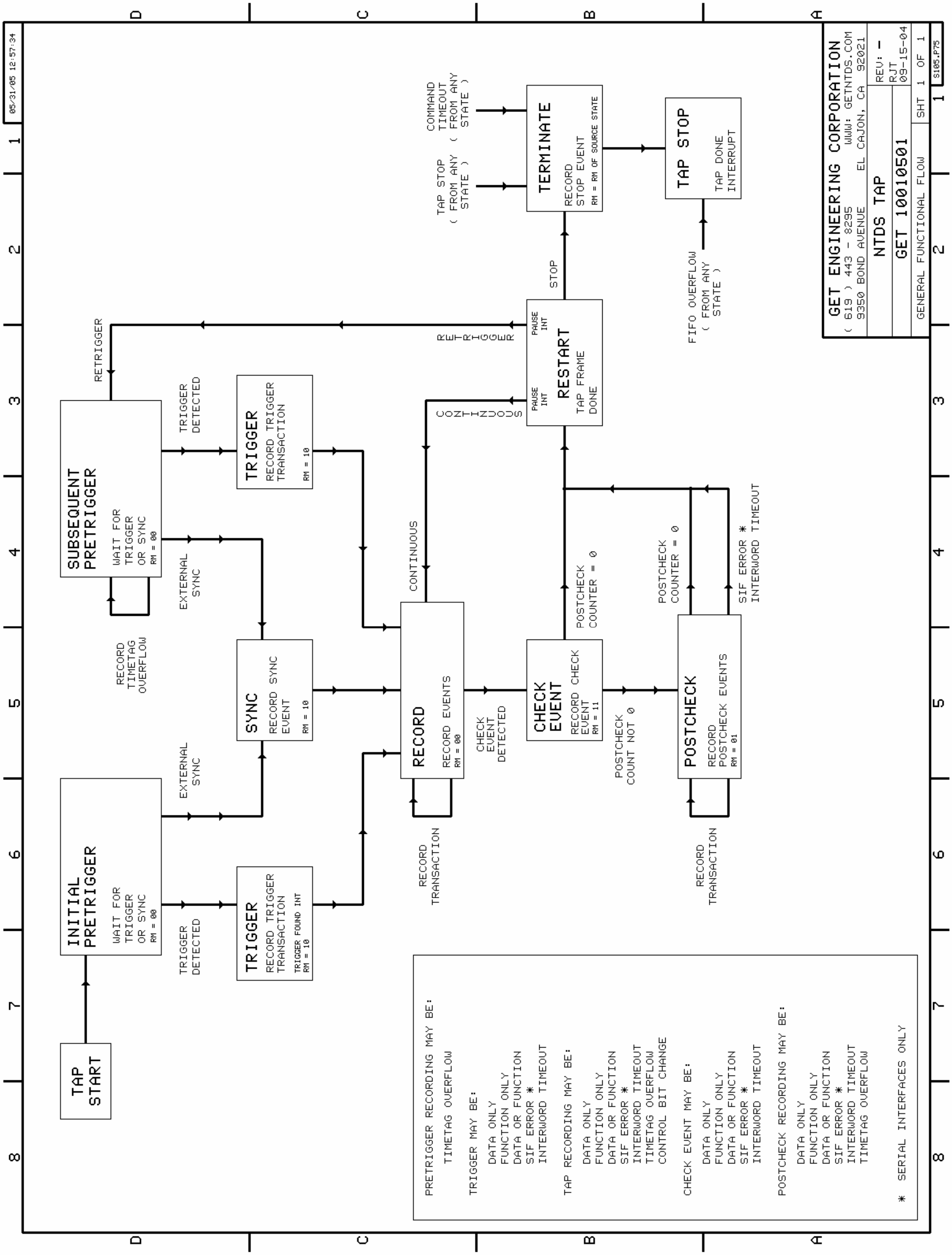
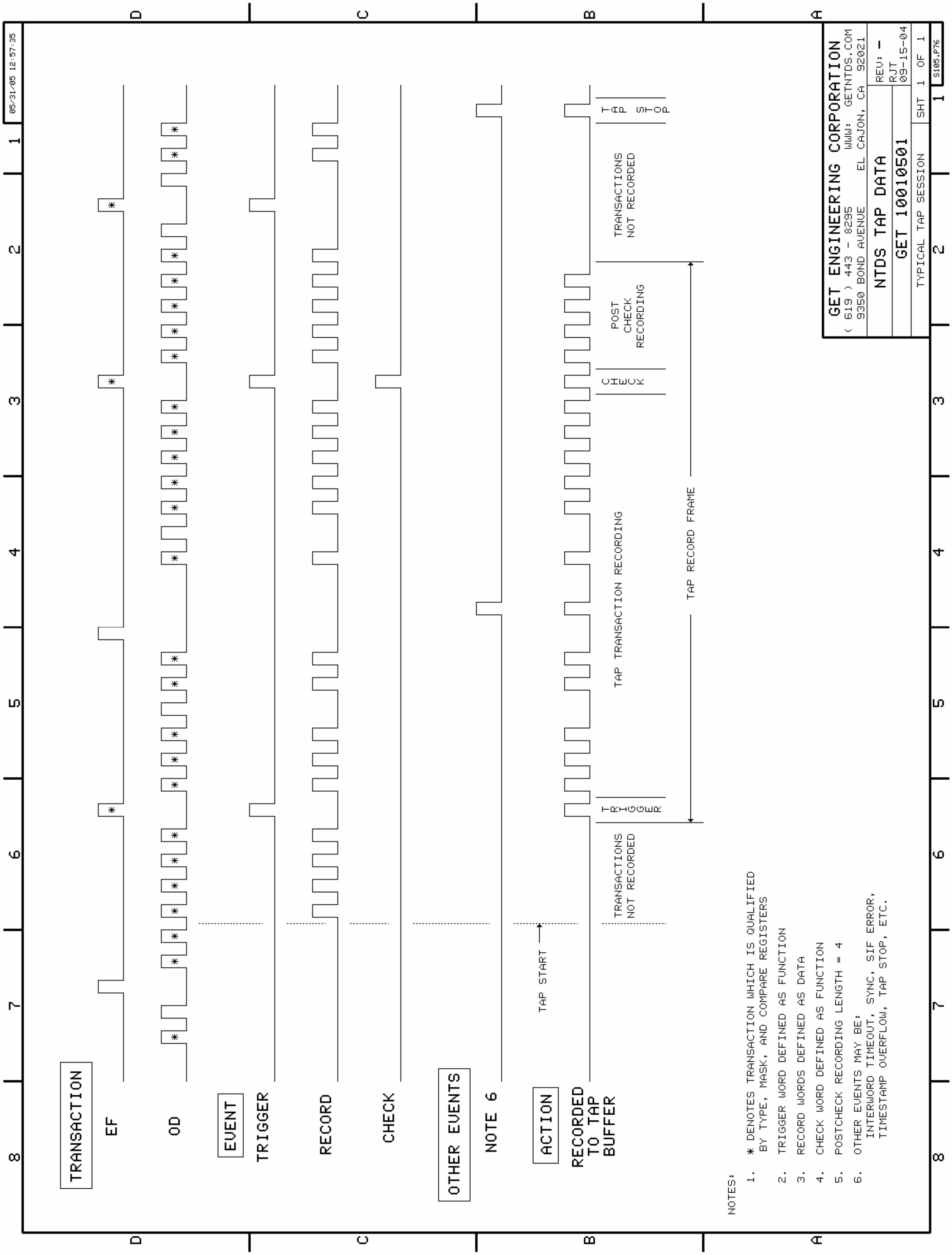


FIGURE 7.6

NTDS TAP RECORDING SESSION



7.5 NTDS SERIAL CHANNEL OPERATION

An NTDS Serial channel consists a Sink and a Source Port, each of which transacts 32 bit information and 3 or 4 bit control frames. The transfer of serial information frames is controlled by the operation the control frames. The operation of these NTDS channels is described in detail in other sections of this document. For a complete description of NTDS serial data exchange protocols refer to MIL-STD-1397C (SHIPS) Military Standard Document.

7.5.1 SERIAL CHANNEL TAP OPERATION

The Sink and Source Ports can be used to passively record transactions between two other NTDS devices. The serial TAP it records transactions based on the presence of SWT or Burst IFs. The SIS and SOS control frames are used only in the evaluation of SIF errors. Control frame formats, IF parity, and timing parameters can be specified by the user. Transaction information is collected after the entire IF is received (Figure 7.8).

7.6 TAP EVENT DETECTION

The TAP operation is controlled by a set of registers which define the operating parameters for performing transaction and event detection and recording. Among these registers are the interword and buffer timers, and the Trigger, Record, and Check mask registers.

7.6.1 TRIGGER COMPARE AND MASK

The Trigger Compare and Mask Registers specify the data field portion of the TAP trigger event. All detected transactions are tested to see if they satisfy the defined trigger condition. This evaluation criteria includes transfer type and data field pattern matching. A trigger condition exists and transaction recording can begin if a type and data field match are found. The set bits in the Trigger Mask Register specify which bits in the Trigger Compare Register will be used when performing the data field pattern match.

7.6.2 RECORD COMPARE AND MASK

The Record Compare and Mask Registers specify the data field TAP recording filter. This filter is used during all Record and Post-termination recording operations. All detected transactions are tested to see if they satisfy the defined recording conditions. This evaluation criteria includes transfer type and data field pattern matching. A recording condition exists if a type and data field match are found. The set bits in the Record Mask Register specify which bits in the Record Compare Register will be used when performing the data field pattern match.

7.6.3 CHECK COMPARE AND MASK

The Check Compare and Mask Registers specify the data field data field portion of the TAP check event. All detected transactions are tested to see if they satisfy the defined check conditions. This evaluation criteria includes transfer type and data field pattern matching. A check condition exists and Post-check transaction recording can begin if a type and data field match are found. The set bits in the Check Mask Register specify which bits in the Check Compare Register will be used when performing the data field pattern match.

7.7 TAP TIMEOUTS

The TAP contains several timers which provide event detection based on several timeout conditions. When specified, the timeout events are recorded into the TAP buffer. Additionally, the timeout events can also specify a TAP termination condition. The operation of these timeouts are illustrated in the TAP Functional Flow Diagram, Figure 7.6.

7.7.1 COMMAND TIMEOUT

The Command Timer is 32 bit counter based on a 1 microsecond clock and provides a method of terminating the TAP after a specified period has expired. The Command timer can optionally be configured as a Buffer period timer. The Command Timer is initialized with the specified timeout period and started when the TAP is started. When configured as a Buffer timer the counter is started after the first NTDS transaction is detected after the TAP is started. If the Command Timer expires before any other defined terminating condition is detected, the TAP session will be terminated, regardless of operational state.

7.7.2 INTERWORD TIMEOUT

The Interword Timer is 16 bit counter based on a selectable 1 microsecond or 1 millisecond clock. An Interword Timeout event can be specified to terminate a current Record or Post-terminate recording operation. The interword timer is initialized and started when a transaction is detected. An interword timeout is declared if this timer expires before the next transaction is detected. When the interword timeout occurs a TAP event is recorded and the TAP frame or recording session can be optionally stopped.

7.7.3 SIF ERRORS

The Serial Interface adaptors can be configured to generate a TAP recording event when a SIF error (IF format, control frame format, or protocol sequence) is detected. The actual control frames are not recorded and the SIF error event is reported in the Status Byte and timestamp fields of the recording word. A protocol sequence error is declared if consecutive control frames with the same ID bits are detected. Additionally, a SIF recording event will be declared if an IF error (framing, sync, or parity) or control frame error (framing or sync) is detected. The TAP frame or recording session can be terminated when a SIF error is detected.

7.8 TAP EVENT RECORDING

All TAP events are recorded in the order in which they are received. The timestamp is reset after each event is recorded and represents the time elapsed since the previously recorded TAP event. A typical TAP recording session is depicted in Figure 7.6. The typical TAP recording session buffer may contain of one or more TAP Recording Frames, depending upon selected retrigger and termination options. Each TAP Recording Frame consists of a number of a detected trigger transaction and/or an external synch event, a number of recorded transactions and TAP events, a possible check transaction or event, a possible number of post-check transactions and events, and a TAP stop/restart event word.

TABLE 7.1

CONFIGURATION OPTIONS

PARALLEL INTERFACE ADAPTOR OPTIONS		
OPTION	MNEMONIC	DESCRIPTION
NTDS CATEGORY	INPUT	TAP CPU INPUT FROM PERIPHERAL INTERFACE
	OUTPUT	TAP CPU OUTPUT TO PERIPHERAL INTERFACE
NTDS TYPE	SLOW	NTDS SLOW (-15 VOLT NOM) OPERATION
	FAST	NTDS FAST (-3 VOLT NOM) OPERATION
	ANEW/H	NTDS ANEW OR TYPE H (+3 VOLT NOM) OPERATION
TYPE E - SERIAL INTERFACE ADAPTOR OPTIONS		
OPTION	MNEMONIC	DESCRIPTION
PARITY	ODD	SERIAL DATA PARITY IS ODD
	EVEN	SERIAL DATA PARITY IS EVEN
	NONE	SERIAL DATA HAS NO PARITY BIT
CONTROL FRAME	SIS ID	0 OR 1
	SOS ID	0 OR 1
SIF	SIFEN	1 = SIF TESTING ENABLED. 0 = DISABLED
TYPE D - SERIAL INTERFACE ADAPTOR OPTIONS		
OPTION	MNEMONIC	DESCRIPTION
NONE		ERROR TESTING AVAILABLE FOR TYPE D ADAPTORS

FIGURE 7.7

PARALLEL CHANNEL TAP TIMING

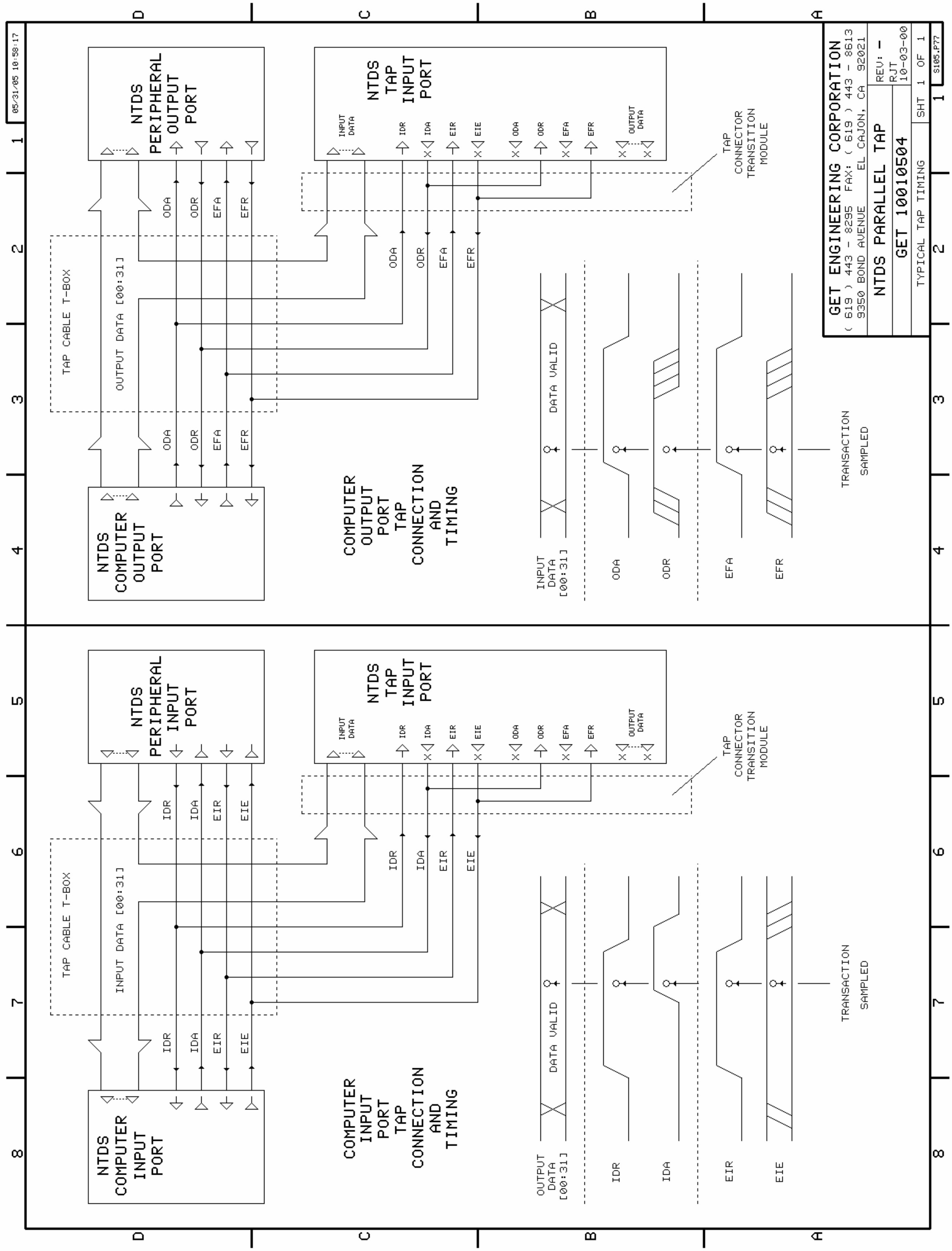
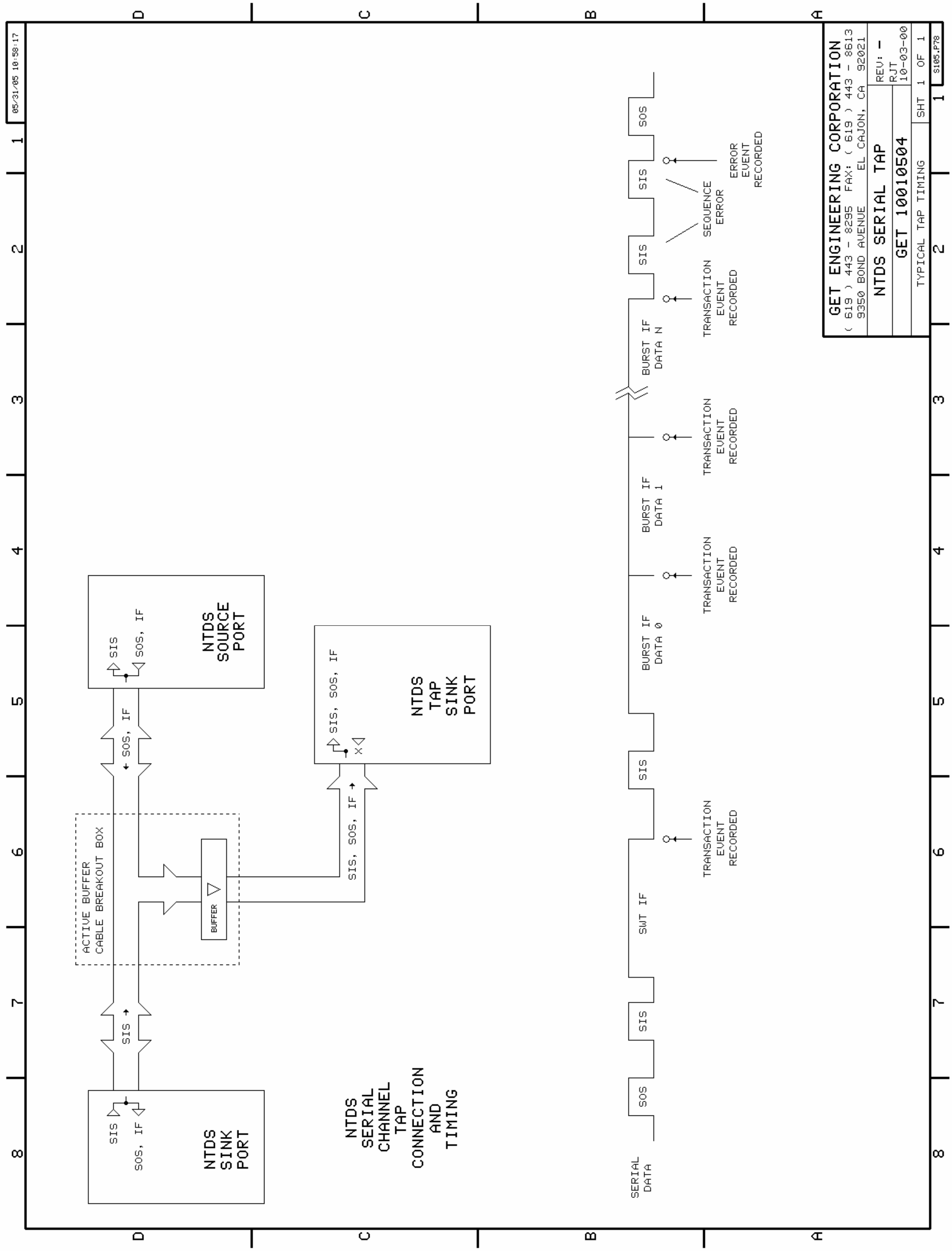


FIGURE 7.8

SERIAL CHANNEL TAP TIMING



SECTION 8
NTDS INTERFACE
CONNECTORS AND CABLES

8.1 NTDS CABLES

The maximum cable length allowed depends on the cable and the interface type (Table 8.1). The maximum lengths indicated are those for which proper operation is assured for equipment otherwise fully conforming to the NTDS specification. The interface circuits used in GET NTDS interface adaptors are designed to support much longer cable lengths. However, each system interface must be individually analyzed for proper operation with longer cables. Issues regarding buffer timeouts, transaction interword timeouts, and other possible problems caused by the additional delays caused by longer cables must be addressed. The following description of NTDS cables and connectors is intended only as an aid in explaining possible interconnection schemes and does not cover all aspects of NTDS connectivity. For a complete description of NTDS cables and connectors refer to MIL-STD-1397C (NAVY) Military Standard Document.

8.1.1 INDUSTRY STANDARD CABLES

Due to the high cost and relatively long lead times for LS2U-45 shipboard cable many shore based or development NTDS installations are opting for the use of commercial cable equivalents. However, under most conditions commercial cable is not recommended for shipboard installations. GET produces a commercial grade cable that has equivalent electrical characteristics as the 2U cable. This 37 conductor pair, PVC jacketed cable has the advantage of being highly flexible while maintaining a 100% metal braid shield, and a mylar foil shield with open drain wire and is completely suitable for most NTDS applications. Complete specifications for the GET 46523437 cable are shown in Figure 8.1.

8.2 NTDS CONNECTORS

The connectors used on NTDS parallel interface systems are keyed to prevent improper connection. By convention the references to input and output are with respect to the computer. The computer input cabinet connector may be the same as the peripheral equipment output cabinet connector. The computer output cabinet connector may be the same as the peripheral equipment input cabinet connector. This configuration, if the same family of connectors is used, allows the Input cables to be interchanged with the Output cables by turning them end for end. The recommended cabinet and cable connectors are listed in Table 8.2.

8.2.1 INDUSTRY STANDARD PARALLEL CONNECTORS

Commercial ribbon cable systems are typically used for most development and shore based systems. Ribbon cables are not recommended for shipboard installations. GET produces a complete line of transition modules that allow quick ribbon cable connections to NTDS devices. These compact modules feature high density 80 contact ribbon cable connectors which are compatible with all GET NTDS products. These easily interchangeable cable transition modules enable efficient system reconfiguration and troubleshooting.

8.2.2 INDUSTRY STANDARD SERIAL CONNECTORS

The physical requirements placed on most commercial interface adaptors require the use of relatively small connectors. The large NTDS serial interface coax and triax connectors are typically too large to fit in most commercially packaged computer systems. This has led the industry to shift to smaller electrically equivalent connectors, as listed in Table 8.2.

8.3 NTDS CONNECTOR SIGNAL ASSIGNMENTS

The standard function to connector pin assignments for the connectors listed in Table 8.2 are listed in Table 8.3. Pins not listed may have no connections. The standard cable wire pair color code must be used to facilitate connector maintenance and guarantee signal integrity.

8.4 ATDS CONNECTOR SIGNAL ASSIGNMENTS

A front panel mounted 25 contact connectors are used as the ATDS serial interface for standard GET ATDS products. The connectors used and their recommended mating cable connector are listed below. Unless otherwise specified, the GET ATDS interface features bidirectional transceivers. These transceivers are configured as drivers or receivers, depending on the operating mode (DTS or TDS CPU). Unused signals should be left open (not connected). The signal pin assignments and the transceiver modes for the ATDS interface connector are listed in Table 8.4.

QUALITY	**MANUFACTURER**	**FRONT PANEL SOCKET CONNECTOR**	**MATING CABLE PLUG CONNECTOR** W / 18" WIRED LEADS	**MATING CABLE PLUG CONNECTOR** SOLDER / CRIMP
Commercial	CANNON	DB25-S	-	DB25-P S
Commercial	CANNON	MDSM-25SC-Z10-VR17	CA111972-12	MDSM-25SC-Z11-VS1 C
Commercial	MOLEX	83614-9012	83424-9019	83424-9014 C
Military	CANNON	MDM-25SBRP-T	M83513/03D01C	M83513/01DC S

TABLE 8.1

MAXIMUM NTDS CABLE LENGTHS

INTERFACE TYPE	NTDS CABLE TYPE	
PARALLEL INTERFACE SYSTEMS		
	2U OR 2UW OR LS2U	2AU OR 2AUW OR LS2AU
A	300 FT 91.4 METERS	300 FT 91.4 METERS
B	50 FT 15.2 METERS	150 FT 45.7 METERS
C	100 FT 30.5 METERS	250 FT 76.2 METERS
H	100 FT 30.5 METERS	250 FT 76.2 METERS
SERIAL INTERFACE SYSTEMS		
	RG/12A	
D	1000 FT 304.8 METERS	
	MIL-C-17/135 TRF-8	MIL-C-17/134 TRF-58
E	985 FT 300 METERS	395 FT 120 METERS

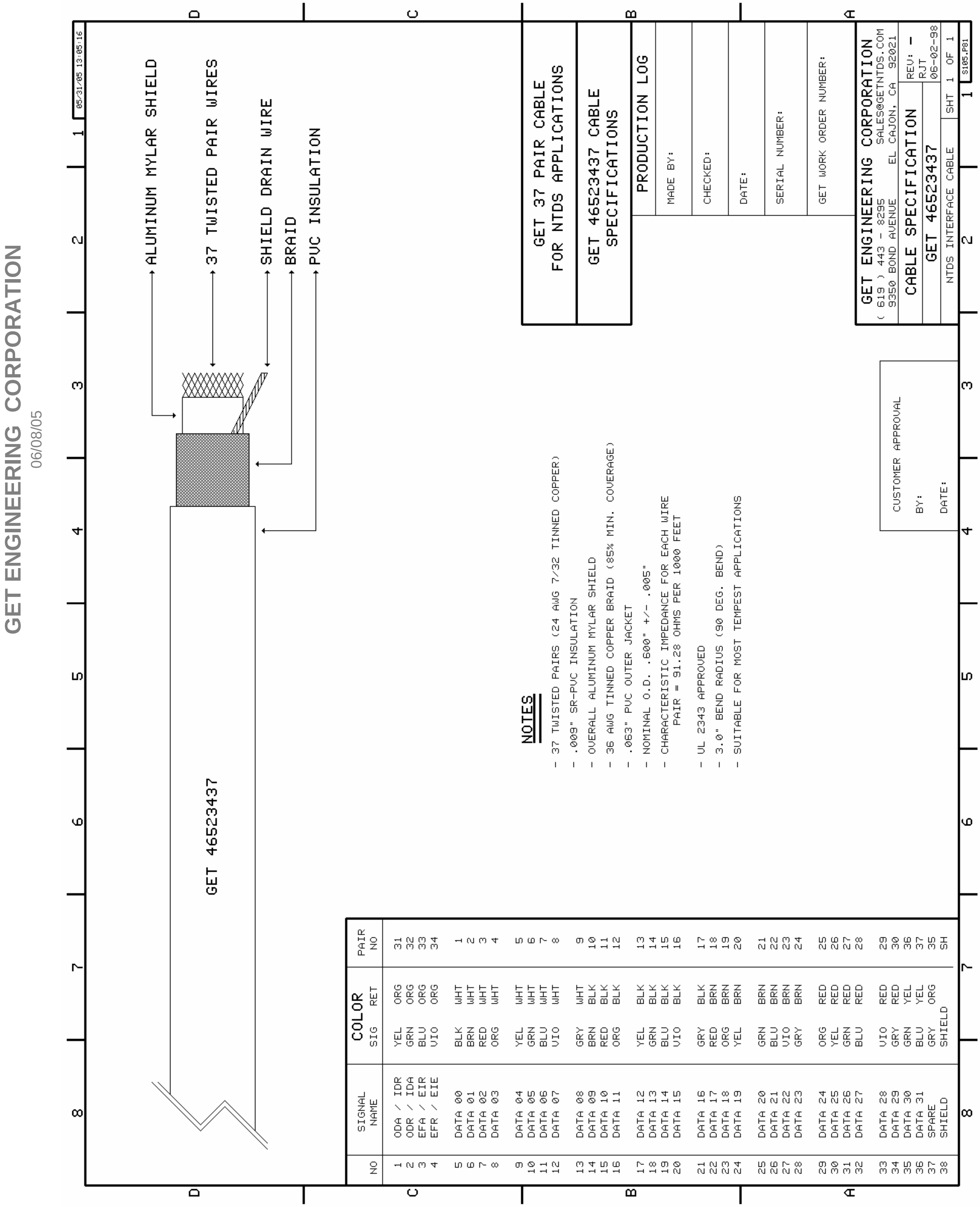
TABLE 8.2

NTDS CONNECTORS

NTDS TYPE	COMMON NAME	NUMBER OF CONTACTS	PORT	CABINET CONNECTOR	CABLE CONNECTOR
A, B, C, H	UYK/20	120	INPUT	GET 45121120	7101943-02
			OUTPUT	GET 45121121	7101943-01
A, B, C, H	UYK/43	92	INPUT	M28840/12AG1P1	M28840/16AG1S1
			OUTPUT	M28840/12AG1P2	M28840/16AG1S2
A, B, C, H	DPD90 CP-642	90	INPUT	DPD-90-34P	DPD-90-33S
			OUTPUT	DPD-90-34P	DPD-90-33S
A, B, C, H	UYK/7	85	INPUT	M81511/01EF01P1	M81511/06EF01S1
			OUTPUT	M81511/01EF01P2	M81511/06EF01S2
A, B, C, H	UYK/44	79	INPUT	D38999/20WG35PN	D38999/26WG35SN
			OUTPUT	D38999/20WG35PA	D38999/26WG35SA
D	SERIAL	COAX	MIL		
			COMMERCIAL	UCBBJR-26	PL20-7
E	LOW LEVEL SERIAL	TRIAX	MIL		M49141/1-0001
			MIL	M49142/2-0001	M49141/1-0002
			COMMERCIAL	BJ-77	PL75C-7
			COMMERCIAL	BJ-80	PL80-7

FIGURE 8.1

GET CABLE SPECIFICATION



NO	SIGNAL NAME	COLOR SIG	COLOR RET	PAIR NO
1	ODA / IDR	YEL	ORG	31
2	ODR / IDA	GRN	ORG	32
3	EFA / EIR	BLU	ORG	33
4	EFR / EIE	VIO	ORG	34
5	DATA 00	BLK	WHT	1
6	DATA 01	BRN	WHT	2
7	DATA 02	RED	WHT	3
8	DATA 03	ORG	WHT	4
9	DATA 04	YEL	WHT	5
10	DATA 05	GRN	WHT	6
11	DATA 06	BLU	WHT	7
12	DATA 07	VIO	WHT	8
13	DATA 08	GRY	WHT	9
14	DATA 09	BRN	BLK	10
15	DATA 10	RED	BLK	11
16	DATA 11	ORG	BLK	12
17	DATA 12	YEL	BLK	13
18	DATA 13	GRN	BLK	14
19	DATA 14	BLU	BLK	15
20	DATA 15	VIO	BLK	16
21	DATA 16	GRY	BLK	17
22	DATA 17	RED	BRN	18
23	DATA 18	ORG	BRN	19
24	DATA 19	YEL	BRN	20
25	DATA 20	GRN	BRN	21
26	DATA 21	BLU	BRN	22
27	DATA 22	VIO	BRN	23
28	DATA 23	GRY	BRN	24
29	DATA 24	ORG	RED	25
30	DATA 25	YEL	RED	26
31	DATA 26	GRN	RED	27
32	DATA 27	BLU	RED	28
33	DATA 28	VIO	RED	29
34	DATA 29	GRY	RED	30
35	DATA 30	GRN	YEL	36
36	DATA 31	BLU	YEL	37
37	SPARE	GRY	ORG	35
38	SHIELD	SHIELD		SH

TABLE 8.3

MIL-STD-1397 (NAVY) CABLE PIN ASSIGNMENTS

05/31/05 13:13:42

STANDARD GET PRODUCT CONNECTORS

CONNECTOR		3-M		MOLEX				AMPHENOL		DUPONT			
CABLE OUTPUT		3425-6650		52758-1200				845-C0 80SALA00		50357-5112A			
CABLE INPUT		3414-6634											
PANEL OUTPUT		3433-5302		52755-1200				845-B0 80PALA00		50576-5112F			
PANEL INPUT		3431-5302											
DENSITY →		50 PIN		120 PIN TRANS		RECV		80 PIN		112 PIN TRANS		RECV	
NO	SIGNAL	SIG	RET	SIG	RET	SIG	RET	SIG	RET	SIG	RET	SIG	RET
1	SHIELD		1		SH		SH		1				
2	ODA / IDR	3	4	5	1	53	49	3	4	B01	A01	D01	C01
3	ODR / IDA	5	6	6	2	54	50	5	6	B02	A02	D02	A01
4	EFA / EIR	7	8	7	3	55	51	7	8	B03	A03	D03	C03
5	EFR / EIE	9	10	8	4	56	52	9	10	B04	A04	C02	A03
6	DATA 00	17	18	13	25	61	57	13	14	A05	A16	D04	C04
7	DATA 01	19	20	9	25	62	58	15	16	A06	A16	D05	C05
8	DATA 02	21	22	14	25	63	59	17	18	A07	A16	D06	C06
9	DATA 03	23	24	10	25	64	60	19	20	B07	A16	B05	B06
10	DATA 04	25	26	15	26	69	65	21	22	A08	A16	D07	C07
11	DATA 05	27	28	11	26	70	66	23	24	A09	A16	D08	C08
12	DATA 06	29	30	16	26	71	67	25	26	A10	A16	D09	C09
13	DATA 07	31	32	12	26	72	68	27	28	B10	A16	B08	B09
14	DATA 08	15	16	21	27	77	73	29	30	A11	A16	D10	C10
15	DATA 09	13	14	17	27	78	74	31	32	A12	A16	D11	C11
16	DATA 10	35	36	22	27	79	75	33	34	A13	A16	D12	C12
17	DATA 11	37	38	18	27	80	76	35	36	B13	A16	B11	B12
18	DATA 12	39	40	23	28	85	81	37	38	A14	A16	D13	C13
19	DATA 13	41	42	19	28	86	82	39	40	B14	A16	D14	C14
20	DATA 14	43	44	24	28	87	83	41	42	A15	A16	D15	C15
21	DATA 15	45	46	20	28	88	84	43	44	B15	A16	D16	C16
22	DATA 16	1	2	37	29	93	89	47	48	A17	A28	D17	C17
23	DATA 17	3	4	33	29	94	90	49	50	A18	A28	D18	C18
24	DATA 18	5	6	38	29	95	91	51	52	B18	A28	B16	B17
25	DATA 19	7	8	34	29	96	92	53	54	A19	A28	D19	C19
26	DATA 20	9	10	39	30	101	97	55	56	A20	A28	D20	C20
27	DATA 21	11	12	35	30	102	98	57	58	A21	A28	D21	C21
28	DATA 22	13	14	40	30	103	99	59	60	B21	A28	B19	B20
29	DATA 23	15	16	36	30	104	100	61	62	A22	A28	D22	C22
30	DATA 24	19	20	45	31	109	105	63	64	A23	A28	D23	C23
31	DATA 25	21	22	41	31	110	106	65	66	A24	A28	D24	C24
32	DATA 26	23	24	46	31	111	107	67	68	B24	A28	B22	B23
33	DATA 27	25	26	42	31	112	108	69	70	A25	A28	D25	C25
34	DATA 28	27	28	47	32	117	113	71	72	A26	A28	D26	C26
35	DATA 29	29	30	43	32	118	114	73	74	A27	A28	D27	C27
36	DATA 30	31	32	48	32	119	115	75	76	B27	A28	B25	B26
37	DATA 31	33	34	44	32	120	116	77	78	B28	A28	D28	C28
		34 PIN											

MIL-STD-1397C SPECIFIED CONNECTORS

CONNECTOR		DPD-90-		D38999\		M81511\		M28840\		UNISYS	
CABLE OUTPUT		33S		26WG35SA		06EF01S2		16AG1S2		7101943-01	
CABLE INPUT				26WG35SN		06EF01S1		16AG1S1		7101943-02	
PANEL OUTPUT		34P		20WG35PA		01EF01P2		10AG1P2		GET 45121121	
PANEL INPUT				20WG35PN		01EF01P1		10AG1P1		GET 45121120	
DENSITY		90 PIN		79 PIN		85 PIN		92 PIN		120 PIN	
NO	SIGNAL	SIG	RET	SIG	RET	SIG	RET	SIG	RET	SIG	RET
1	SHIELD		45		7		74		6		B-01
2	ODA / IDR	1	11	79	78	1	6	1	7	B-05	A-05
3	ODR / IDA	2	12	77	76	2	7	2	8	B-06	A-06
4	EFA / EIR	3	13	75	74	3	8	3	9	B-07	A-07
5	EFR / EIE	4	14	73	72	4	9	4	10	B-08	A-08
6	DATA 00	9	19	71	70	13	21	14	23	D-01	C-01
7	DATA 01	10	20	69	68	14	22	15	24	D-02	C-02
8	DATA 02	22	33	67	66	15	23	16	25	D-03	C-03
9	DATA 03	23	34	65	64	16	24	17	26	D-04	C-04
10	DATA 04	24	35	63	62	17	25	18	27	D-05	C-05
11	DATA 05	25	36	61	60	18	26	19	28	D-06	C-06
12	DATA 06	26	37	59	58	29	39	33	42	D-07	C-07
13	DATA 07	27	38	57	56	30	40	34	43	D-08	C-08
14	DATA 08	28	39	55	54	31	41	35	44	D-09	C-09
15	DATA 09	29	40	53	52	32	42	36	45	D-10	C-10
16	DATA 10	30	41	51	50	33	43	37	46	D-11	C-11
17	DATA 11	31	42	49	48	34	44	38	47	D-12	C-12
18	DATA 12	32	43	47	46	35	45	39	48	G-01	H-01
19	DATA 13	47	58	45	44	36	46	40	49	G-02	H-02
20	DATA 14	48	59	43	42	37	47	41	50	G-03	H-03
21	DATA 15	49	60	41	40	49	58	52	61	G-04	H-04
22	DATA 16	50	61	39	38	50	59	53	62	G-05	H-05
23	DATA 17	51	62	37	36	51	60	54	63	G-06	H-06
24	DATA 18	52	63	35	34	52	61	55	64	G-07	H-07
25	DATA 19	53	64	33	32	53	62	56	65	G-08	H-08
26	DATA 20	54	65	31	30	54	63	57	66	G-09	H-09
27	DATA 21	55	66	29	28	55	64	58	67	G-10	H-10
28	DATA 22	56	67	27	26	56	65	59	68	G-11	H-11
29	DATA 23	57	68	25	24	57	66	60	69	G-12	H-12
30	DATA 24	70	80	23	22	67	75	71	80	J-01	K-01
31	DATA 25	71	81	21	20	68	76	72	81	J-02	K-02
32	DATA 26	72	82	19	18	69	77	73	82	J-03	K-03
33	DATA 27	73	83	17	16	70	78	74	83	J-04	K-04
34	DATA 28	74	84	15	14	71	79	75	84	J-05	K-05
35	DATA 29	75	85	13	12	72	80	76	85	J-06	K-06
36	DATA 30	76	86	11	10	73	81	77	86	J-07	K-07
37	DATA 31	77	87	9	8	5	12	78	87	J-08	K-08
		CP-642		UYK-44		UYK-7		UYK-43		UYK-20	

NTDS CABLES & COLOR CODES

NO	LS2U45 TYPE LENGTH			MIL-STD-1397C			LS2AU45 TYPE LENGTH
	A 300			MIL-C-24643			A 300
	B 50			← MAXIMUM CABLE → RECOMMENDED LENGTHS (FT)			B 100
	C/H 100						C/H 250
	GET 46523437			LS2U45 / LS2AU45			← CABLE
	37 PAIR			45 PAIR			←DENSITY
	SIG	RET	PR #	SIG	RET	PR #	SIGNAL
1		SH	SH		SH	SH	SHIELD
2	YEL	ORG	31	ORG	BRN	40	ODA / IDR
3	GRN	ORG	32	ORG	BLU	39	ODR / IDA
4	BLU	ORG	33	GRN	PNK	38	EFA / EIR
5	VIO	ORG	34	GRN	TAN	37	EFR / EIE
6	BLK	WHT	1	WHT	BLU	15	DATA 00
7	BRN	WHT	2	WHT	ORG	14	DATA 01
8	RED	WHT	3	RED	BLU	24	DATA 02
9	ORG	WHT	4	WHT	PNK	21	DATA 03
10	YEL	WHT	5	WHT	TAN	20	DATA 04
11	GRN	WHT	6	WHT	YEL	18	DATA 05
12	BLU	WHT	7	WHT	VIO	19	DATA 06
13	VIO	WHT	8	BLK	GRY	7	DATA 07
14	GRY	WHT	9	BLK	WHT	1	DATA 08
15	BRN	BLK	10	BLK	BRN	6	DATA 09
16	RED	BLK	11	BLK	BLU	5	DATA 10
17	ORG	BLK	12	WHT	GRN	13	DATA 11
18	YEL	BLK	13	GRN	GRY	34	DATA 12
19	GRN	BLK	14	RED	BRN	25	DATA 13
20	BLU	BLK	15	RED	GRN	22	DATA 14
21	VIO	BLK	16	BLK	RED	2	DATA 15
22	GRY	BLK	17	BLK	YEL	8	DATA 16
23	RED	BRN	18	BLK	VIO	9	DATA 17
24	ORG	BRN	19	BLK	GRN	3	DATA 18
25	YEL	BRN	20	BLK	ORG	4	DATA 19
26	GRN	BRN	21	BLK	TAN	10	DATA 20
27	BLU	BRN	22	BLK	PNK	11	DATA 21
28	VIO	BRN	23	WHT	RED	12	DATA 22
29	GRY	BRN	24	GRN	BRN	33	DATA 23
30	ORG	RED	25	RED	GRY	26	DATA 24
31	YEL	RED	26	RED	YEL	27	DATA 25
32	GRN	RED	27	RED	ORG	23	DATA 26
33	BLU	RED	28	RED	VIO	28	DATA 27
34	VIO	RED	29	RED	TAN	29	DATA 28
35	GRY	RED	30	RED	PNK	30	DATA 29
36	GRN	YEL	31	GRN	ORG	31	DATA 30
37	BLU	YEL	32	GRN	BLU	32	DATA 31

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GET NTDS I/O STANDARD
FROM MIL-STD-1397C
STANDARD NTDS CONNECTORS

REV: C
RJT
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S105.P82

TABLE 8.4

ATDS CONNECTOR PIN ASSIGNMENTS

SIGNAL NAME	SIGNAL	RETURN	DTS MODE	TDS MODE	CIRCUIT TYPE
SHIELD	1				
FRAME	14	2	DRIVER	RECEIVER	TRANSFORMER
INCOMING DATA	15	3	DRIVER	RECEIVER	TRANSFORMER
OUTGOING DATA	16	4	RECEIVER	DRIVER	TRANSFORMER
DATA CLOCK	17	5	RECEIVER	DRIVER	TRANSFORMER
ADDRESS DATA	18	6	RECEIVER	DRIVER	TRANSFORMER
ADDRESS CLOCK	19	7	RECEIVER	DRIVER	TRANSFORMER
NET CONTROL	8	20	DRIVER	RECEIVER	10 VOLT
SIDETONE FRAME	9	21	DRIVER	RECEIVER	TTL
SIDETONE DATA	10	22	DRIVER	RECEIVER	TTL
SIDETONE CLOCK	11	23	RECEIVER	DRIVER	TTL
NO CONNECTION	12	24			
NO CONNECTION	13	25			

NOTES: CIRCUIT TYPES

TRANSFORMER = 6 VOLT P/P, 100 OHM LOAD - TRANSFORMER COUPLED
10 VOLT = 10 VOLT DC INTERFACE - DIRECT CONNECTION
TTL = TTL LOGIC LEVEL - DIRECT CONNECTION